Board Module

For Xilinx

Spartan-II or Virtex-E

FPGA Families

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EVALXC2S/XCV/XCVE User Manual

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	EVALXCV	Version 1.0	September 2000
	EVALXCVE	Version 1.0	September 2000

This manual describes the technical properties and the usage of the following products:

2.5V Versions:	EVALXCV-HQ240 with XCV50 – XCV800	Version 1.0	September 2000
	EVALXC2S-PQ208 with XC2S50 – XC2S200	Version 1.0	September 2000
1.8V Versions:	EVALXCVE-HQ240 with 50E – 1000E FPGA	Version 1.0	September 2000

Important Note:

The EVALXC2S/XCV/XCVE board module series has been designed and tested exclusively for the usage as a development tool. In particular, strong electromagnetic radiation may be produced. ErSt Electronic GmbH does not undertake any liability for damages that may result from an improper use of this product.

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Notational Conventions:

1. Names of active low signals are marked with a trailing \ or start with x, e.g. CS\ or XCS.
2. When used to describe signal voltage levels, 0 means low voltage, 1 means high voltage.
3. Table and figure references are printed in an italic font.
4. Signal names within a sentence are printed in an italic font.

Abbreviations:

ASIC	Application Specific Integrated Circuit
DIL	Dual Inline
DIP	Dual Inline Package
DLL	Delay-Locked Loop
FPGA	Field Programmable Gate Array
GND	System Ground
HQ	Thermally enhanced QFP
IEEE	Institute of Electrical and Electronics Engineers
IOB	Input/Output Block
ISP	In System Programmable
JTAG	Joint Test Action Group
LED	Light Emitting Diode
OTP	One Time Programmable
PC	Personal Computer
PCB	Printed Circuit Board
PLCC	Plastic Leaded Chip Carrier
PLL	Phase Locked Loop
PROM	Programmable Read Only Memory
PWM	Pulse Width Modulation
QFP	Quad Flat Pack
SCP	Serial Configuration PROM
SMD	Surface Mounted Device
SPROM	Serial PROM
VCCINT	Internal supply voltage
VCCO	Output driver supply voltage
VCCOPT	Optional supply voltage
VCXO	Voltage Controlled Crystal Oscillator
VQ	Plastic very thin QFP
ZBT	Zero Bus Time

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1 Introduction

This manual describes the specific properties of the board module like power supply, reference voltages, FPGA configuration, clocks, reset, LEDs, DIP switches and I/O signals.

Please take information about the FPGA from the Xilinx literature (see *chapter 4 Literature*). Online information can be found on the Xilinx websites:

http://www.xilinx.com

and

http://www.support.xilinx.com

Information about new products and new developments can be found on the ErSt Electronic Website:

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We will answer as soon as possible, usually within one or two days.

2 Overview

2.1 Key Features

- Download: Master Serial Mode (SPROM with socket), Slave Serial Mode (XChecker header connector), Boundary Scan Mode (JTAG header connector), SelectMAP Mode (header connector)
- Configuration from onboard SCPs: ISP SCPs programmable via JTAG, sockets for OTP SCPs.
- I/O bank reference voltages: Two adjustable VREFs for 8 I/O banks (selectable via jumpers) or eight external voltages (e.g. from power module PWR3)
- Voltage supervisor with reset button
- Two separate crystal oscillators with sockets (DIL8 or DIL14)
- Jumpers to select between internal and external clock sources
- Four SMB connectors next to the FPGA for feeding high frequency clocks
- Two header connectors (two rows with 50 pins each) for I/Os, clocks and control signals
- Two header connectors (one row with 50 pins each) for supply and reference voltages from power module
- Four ground clips
- Two user buttons
- Eight position DIP switch
- Display with eight LEDs
- "Done" LED
- Power LEDs
- Mode jumpers M0 / M1 / M2
- Daisy chain configuration with other board modules possible
- Several boards may be connected to form a stack
- Board size 100mm x 150mm

2.2 Applications

- ASIC Emulation
- Error monitoring and analysis
- Digital PLL circuits
- PWM controller
- Adaptive digital filters
- Signal multiplexers
- Stimuli generators
- High speed encoder/decoder
- Memory controller
- Interface controller

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2.3 Function Description

The board module EVALXC2S/XCV/XCVE is equipped with a member of the Xilinx Spartan-II, Virtex or Virtex-E FPGA family in the PQ208 or HQ-240 package, respectively. This board is especially suited to test digital circuits during the early stages of their development. You can easily attach a logic analyzer an watch the signals in real time. The high count of system gates enables you to implement circuits that reach the complexity of ASICs. The configuration data of the FPGA is downloadable using one of four modes (master serial mode (XChecker), slave serial mode (SPROM), boundary scan mode (JTAG) and SelectMAP mode). The block diagram of *Figure 1* shows the functional blocks of the board.

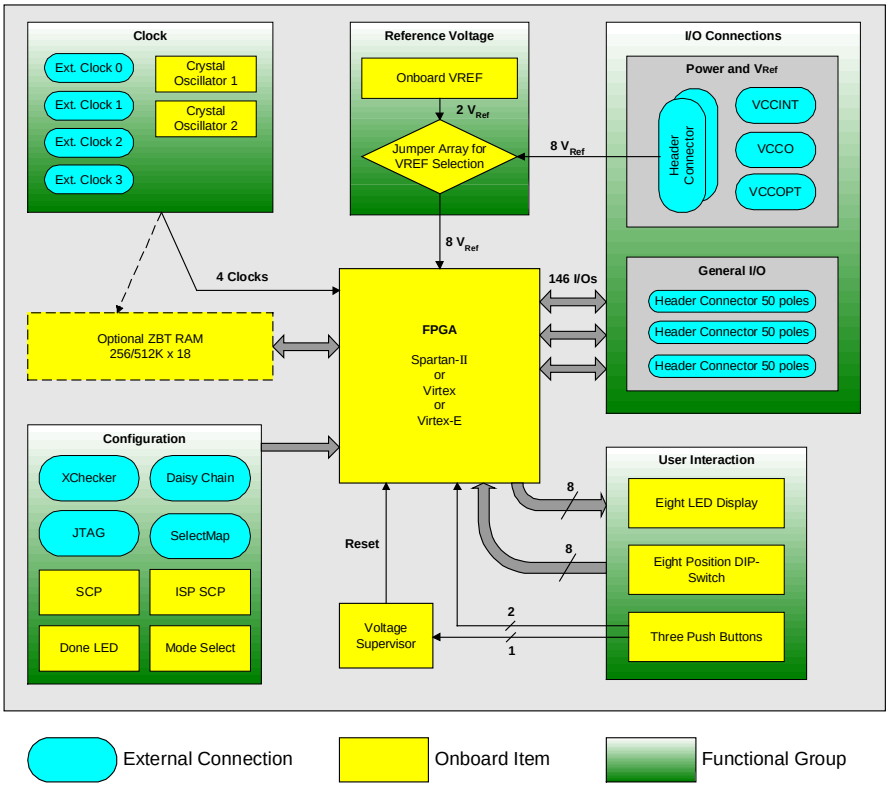

Figure 1: Block diagram of the board module

All general I/Os of the FPGA are routed to header connectors. If you use I/O standards that need reference voltages, you can select up to eight different voltage levels for all eight banks individually with jumpers.

An optional ZBT RAM helps you to support memory-demanding implementations like imaging and telecommunication applications. The clock input of this RAM is connected to the global clock GCK2 of the FPGA to achieve a real synchronous system clock. Alternatively, you can generate the RAM clock internally to the FPGA. In this case the clock is gated through an output pin connected to the RAM clock input via a jumper. The GCK2 clock may then not be driven externally.

By stacking several boards, you may implement circuits whose complexity is beyond the scope of a single FPGA. The whole stack is configurable with a single download by means of an external daisy chain. You can also link the stacked boards in a JTAG chain.

Two sockets are provided to hold Xilinx OTP SCPs (two XC1704L in a PLCC44 package). In addition, two ISP SCPs (XC1800 family) are mounted on the back side of the board. You can program these SCPs using the JTAG mode.

Four clock sources can be used where two of them are either an onboard crystal oscillator or an external source. The other two sources are always external sources. The crystal oscillators are mounted in sockets and can therefore be exchanged easily. Both, a DIL-8 and a DIL-14 package can be used. There is the possibility to terminate all clock traces near the FPGA with resistors to ground. These resistors may be mounted by you on the bottom side of the PCB.

A voltage supervisor circuit generates a short pulse of ca. 2ms duration whenever the core supply voltage (VCCINT) drops below 2.2V (1.7V for Virtex-E) and on power up. The polarity of the reset pulse can be chosen to be either active high or active low. Such a reset pulse is also generated when you press the reset button.

An eight-position DIP switch is available for user specific applications. In addition, there are three push buttons. One of them is intended primarily for use as a reset button and is connected to the voltage supervisor circuit. The other two buttons are available for arbitrary purposes.

A row with eight LEDs may function as a display for status and error messages. You may disconnect these LEDs from the I/O signals by means of jumpers. This is especially useful if you stack several boards and do not want to have the LEDs connected in parallel.

3 Technical Information

This chapter gives a detailed description of the technical details of the board. Please consult the schematic diagrams where you find the components who's designators are mentioned in the text.

3.1 Power Supply

Due to the 0.18/0.22µm process, the FPGA works with an internal supply voltage (VCCINT) of 1.8/2.5V and an output driver voltage (VCCO) of up to max. 3.3V. Depending on the chosen I/O standard, VCCO can be 1.5V, 2.5V or 3.3V. All inputs are 5V compatible. Other devices on the board (crystal oscillators and SCPs) need a supply voltage of 3.3V. This voltage can be derived via a jumper from VCCO if an appropriate I/O standard is used, i.e. one which works with 3.3V. For other I/O standards, which work with 1.5V or 2.5V, the 3.3V voltage must be taken from a third source (VCCOPT).
The voltages VCCINT, VCCO and VCCOPT may be taken from external power supplies via the power connectors. The preferred method, however, is the usage of the power module PWR3 that we developed especially for this purpose. The power module can be plugged onto the Virtex board module by means of two 50-pole connectors. In addition, the power module also generates eight reference voltages needed by the FPGA to support the multi I/O standards. Beside the 50-pole connectors, the power module is equipped with three power connectors and can be connected to other board modules using cables.

Connector	Pin Number	Signal Name
ST6	1 to 12	VCCOPT
	13 to 25	GND
	26 to 42	Reserved
	43	VREF0
	44	VREF1
	45	VREF2
	46	VREF3
	47	VREF4
	48	VREF5
	49	VREF6
	50	VREF7
ST7	1 to 12	VCCINT
	13 to 38	GND
	39 to 50	VCCO

Table 1: Pin assignment on the power header connectors ST6 and ST7

3.1.1 3.3V Supply

A 3.3V supply is needed for various devices (SPROMs, crystal oscillators, voltage supervisor, general purpose LEDs, JTAG and XChecker ports). This supply may be derived from VCCO or VCCOPT according to the following table:

VCCO	VCCOPT	J24 (3.3V)
1.5V	3.3V	1-2
2.5V	3.3V	1-2
3.3V	not used	2-3

Table 2: Derivation of the 3.3V supply voltage

In the case of a VCCO voltage of 3.3V, the VCCOPT voltage is not needed. If the power supply device is a PWR3 power module, its VCCOPT output may be used for arbitrary purposes, e.g. as a 5V power supply.

3.1.2 Reference Voltages

The FPGAs have eight I/O banks, which must be supplied with different reference voltages depending on the used I/O standard. Usually you do not need more than two different I/O standards at one time. For convenience, two different reference voltages are generated on the board, derived from VCCINT using trim potentiometers. In conjunction with the PWR3 power module, the reference voltages should be taken from the PWR3. This way you can operate all eight banks differently.

Trim Potentiometer	Reference Voltage
R56	VREF0 (onboard)
R55	VREF1 (onboard)

Table 3: Trim potentiometer for internal reference voltages

The internal reference voltages can be monitored at the connectors J110 (VREF0) and J111 (VREF1), respectively. Connect a voltmeter to the appropriate port while adjusting the potentiometer.

The choice of a reference voltage source is done using jumpers. To choose an internal reference voltage, you must set the jumpers according to the following table:

Bank	VREF0 onboard	VREF1 onboard
0	J102 (1-2)	
1	J103 (1-2)	
2	J104 (1-2)	
3	J105 (1-2)	
4		J106 (2-3)
5		J107 (2-3)
6		J108 (2-3)
7		J109 (2-3)

Table 4: Choosing an internal reference voltage

When an external reference voltage is used, a dedicated reference voltage can be assigned to each bank. The jumper settings are listed in *Table 5.*

Bank	VREF0	VREF1	VREF2	VREF3	VREF4	VREF5	VREF6	VREF7
0	J101 2-3							
1		J103 2-3						
2			J104 2-3					
3				J105 2-3				
4					J106 1-2			
5						J107 1-2		
6							J108 1-2	
7								J109 1-2

Table 5: Choosing an external reference voltage

3.1.3 Output Driver Supply Voltage

You can connect each of the eight I/O bank's output driver supply to the VCCO voltage individually. To do this, set the jumpers J114 to J121 according to the following table:

Bank	Jumper for connection to VCCO
0	J114
1	J115
2	J116
3	J117
4	J121
5	J118
6	J119
7	J120

Table 6: Connecting the output driver voltage

The VCCO voltage comes from the power module and can be selected to be 1.5V, 2.5V or 3.3V. If you use an I/O standard that does not require an output driver voltage, just remove the corresponding jumper. If you need two or three different output driver voltages at the same time, you can do this be removing the appropriate jumper and using one of the jumper pins to connect an external supply.

3.1.4 Mounting the PWR3 Power Module

The PWR3 power module can be plugged to the board module by means of two single inline 50-pole connector pairs. The assembly is correct if the three four pole output connectors of the power module and the single six-pole supply voltage connector of the board module are on the same side.

Please check that the orientation of the two boards and the output voltage settings of the power module (refer to the PWR3 user manual) are correct before applying power.

3.2 FPGA Configuration

The FPGAs with Virtex architecture support the following four configuration modes:

- Master Serial Mode
- Slave Serial Mode
- SelectMAP mode
- Boundary-scan mode

The configuration pins (M2, M1, M0) select among these modes with the option in each case of having the IOB pins either pulled up or left floating prior to configuration. The selection codes are listed in *Table 7*.

An inserted jumper ties the appropriate pin to ground whereas the pin is pulled high if the jumper is removed. Here and in the following tables, a “Yes” in the jumper column means that the jumper is present whereas a “–“ means that no jumper is plugged in.

Mode	J3 (M2)	J2 (M1)	J1 (M0)	CCLK Direction	Bits	Busy/ Dout	Internal Pullups
Master Serial	Yes	Yes	Yes	Out	1	Yes	No
Boundary Scan	-	Yes	-	N/A	1	No	No
SelectMAP	-	-	Yes	In	8	No	No
Slave Serial	-	-	-	In	1	No	No
Master Serial	-	Yes	Yes	Out	1	Yes	Yes
Boundary Scan	Yes	Yes	-	N/A	1	No	Yes
SelectMAP	Yes	-	Yes	In	8	No	Yes
Slave Serial	Yes	-	-	In	1	No	Yes

Table 7: Setting the configuration modes

3.2.1 Master Serial Mode

In master serial mode, the CCLK output of the FPGA drives a Xilinx Serial PROM that feeds bit-serial data to the DIN input. The FPGA accepts this data on each rising CCLK edge. After the FPGA has been loaded, the data for the next device in a daisy-chain is presented on the DOUT pin after the rising CCLK edge. The preamble is also forwarded to other devices in the daisy chain. SPROM RESET pin is driven by INIT\, and CE\ input is driven by DONE.

The master serial mode is selected by the following jumper settings:

J3 (M2)	J2 (M1)	J1 (M0)	Internal pullups on IOB pins
Yes	Yes	Yes	No
-	Yes	Yes	Yes

Table 8: Master serial mode selection

3.2.1.1 One Time Programmable PROMs

Two sockets for XC1704L devices in a PLCC44 package are available. U6 is the first device in the chain. The CEO\ output of the first device enables the second device after all of its contents has been put out. If your particular FPGA only needs one PROM to hold the configuration bit stream, insert U6 only.

In order to use these devices as the source of serial configuration data, the following jumper settings apply:

J32 (PROM Sel)
2-3

Table 9: Selecting the XC1704 PROMs as serial configuration data source

3.2.1.2 In System Programmable PROMs

The two ISP PROMs (U1 and U2, both in VQ44 package) of the XC1800 family are optional. Depending on the size of the FPGA only one or both of them are needed. These devices are programmable many times over the JTAG port but work otherwise the same as the XC1700 family. If no ISP PROMs are present, the bypass resistor R61 (0 Ω) connects the JTAG data input directly with the FPGA. If only one if the ISP PROMs is used, the resistor R29 (0 Ω) bypasses the second one.

The jumper settings to use these devices as the source of configuration data are as follows:

J32 (PROM Sel)
1-2

Table 10: Selecting the XC1804 ISP PROMs as serial configuration data source

You can program the devices via the JTAG port J5. TDI of U1 is connected directly with the corresponding pin of J5. U2 is chained with U1, i.e. TDI of U2 is connected with TDO of U1. The pin assignment of the JTAG port is listed in *Table 11*.

Pin of JTAG port J5	Signal Name
1	TMS
2	TDI
3	TDO
4	TCK
5	GND
6	3.3V

Table 11: JTAG port pin assignment

3.2.2 Slave Serial Mode

In slave serial mode, the FPGA receives configuration data in bit-serial form from a serial PROM or other source of serial configuration data. An external device, e.g. XChecker cable, generates the download clock. Multiple FPGAs can be daisy-chained for configuration from a single source. After a particular FPGA has been configured, the data for the next device is routed to the DOUT pin.

The slave serial mode is selected by the following jumper settings:

J3 (M2)	J2 (M1)	J1 (M0)	Internal pullups on IOB pins
-	-	-	No
Yes	-	-	Yes

Table 12: Slave serial mode selection

3.2.2.1 Configuration via XChecker Port

In slave serial mode, the serial configuration data comes from the XChecker port J4. Either a parallel or a serial cable may be used. Due to the 3.3V cable supply voltage, we recommend to use an appropriate cable (Xilinx order number: HW-XCH3V). Nevertheless, experiments with 5V cables showed, that these cables work well down to 3V, parallel cables even down to 2V. The circumstances under which a certain cable will work depend on many factors, including the PC used. Whether a cable that is specified for 5V operation will work is not guaranteed.

In any case we strongly recommend using the MultiLinx cable that has the additional advantage of being able to use the USB bus. This brings an enormous increase in download speed.

The jumper settings to use the XChecker port are as follows:

J32 (PROM Sel)
Removed (neither 1-2 nor 2-3 connected)

Table 13: Jumper settings for XChecker configuration

The pin assignments of the XChecker port connector are listed in the following table:

Pin of XChecker port J4	Signal Name
1	PROG\
2	DONE
3	INIT\
4	CCLK
5	DATA
6	3.3V
7	GND

Table 14: XChecker port pin assignment

3.2.3 SelectMAP Mode

The SelectMAP mode is the fastest configuration option. Byte-serial data is written into the FPGA with a BUSY flag controlling the flow of data. An external data source provides a byte stream, CCLK, a Chip Select (CS) signal and a Write signal (WRITE). If BUSY is asserted (High) by the FPGA, the data must be held until BUSY goes Low. Data can also be read using the SelectMAP mode. If WRITE is not asserted, configuration data is read out of the FPGA as part of a readback operation.

The SelectMAP mode is selected by the following jumper settings:

J3 (M2)	J2 (M1)	J1 (M0)	Internal pullups on IOB pins
-	-	Yes	No
Yes	-	Yes	Yes

Table 15: SelectMAP mode selection

The byte-serial data is fed from an external source to the SelectMAP port J6 using the following pin assignments:

Pin of SelectMAP port J6	Signal Name
1	D0
2	D1
3	D2
4	D3
5	D4
6	D5
7	D6
8	D7
9	BUSY/DOUT
10	WRITE\
11	CS\
12	GND

Table 16: SelectMAP port pin assignment

3.2.4 Boundary Scan Mode

In the boundary-scan mode, no non-dedicated pins are required, configuration being done entirely through the IEEE 1149.1 Test Access Port. Configuration and readback is always available. The boundary-scan mode simply locks out the other modes.

The boundary scan mode is selected by the following jumper settings:

J3 (M2)	J2 (M1)	J1 (M0)	Internal pullups on IOB pins
-	Yes	-	No
Yes	Yes	-	Yes

Table 17: Boundary scan mode selection

The pin assignment of the JTAG port J5 is listed in *Table 11*.

3.2.5 Daisy Chain

If several board modules are stacked together, there is the possibility to configure the whole stack at once. To do this, the individual layers must be connected in form of a daisy chain. This is accomplished by connecting appropriate pins of connector J25 (see *Table 18*) externally.

J25 (Connector)	Pin Name
1	DUP
2	D0/DIN
3	BUSY/DOUT
4	DDOWN

Table 18: Pin assignment of daisy chain connector J25

Use the following scheme for the external connections:

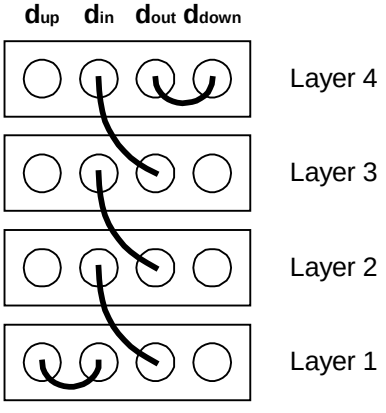

Figure 2: Wiring of the daisy chain

The easiest way to make the connections d_{up}-d_{in} and d_{out}-d_{down} is to insert a jumper. However, these connections are only needed if the stack is connected to a main board and if the configuration data comes from the main board.

If the main board is not used you need only the d_{out}-d_{in} connections. The configuration bit streams are then fed to the lowest layer (SCP or XChecker).

3.3 Clock

All four clock signals (GCK0 to GCK3) are routed to header connectors. *GCK0* and *GCK1* may get the clock signal either from an internal crystal oscillator or from an external source, see *Table 19*.

J26 (GCK0)	J27 (GCK1)	GCK0 Source	GCK1 Source
2-3	2-3	internal U3	internal U4
2-3	1-2	internal U3	external ST4B-54
1-2	2-3	external ST4B-52	internal U4
1-2	1-2	external ST4B-52	external ST4B-54

Table 19: Choice of the clock sources

3.3.1 External Clock

The assignment of the clock signals on the header connectors is listed in 1 FPGA pins for Spartan-II devices are put in parenthesis
Table 20. There is also the possibility to feed the clock via a SMB connector mounted next to the FPGA. This is the preferred method at high clock frequencies.

Signal Name	Connector ST4B	FPGA Pin[1]	Direct Clock Connector (SMB)	Termination Resistor
GCK0	52	92 (80)	J15 (GCK0)	R49
GCK1	54	89 (77)	J16 (GCK1)	R50
GCK2	56	210 (182)	J17 (GCK2)	R51
GCK3	58	213 (185)	J18 (GCK3)	R52

[1] FPGA pins for Spartan-II devices are put in parenthesis

Table 20: External clock signals and termination resistors

3.3.1.1 Termination Resistors

All clock signals may be terminated with resistors (R49 to R52). These are connected immediately from the FPGA pin to ground. These resistors form a parallel termination. The values of the resistors should match the impedance of the circuit board trace having a nominal value of 100 Ohms. Please consider the maximal output current capability of the clock source!

The resistors (SMD, size 0805) can be soldered to the board directly beneath the FPGA on the bottom side of the PCB.

3.3.2 Internal Clock (Crystal Oscillators)

Since the clock frequency depends strongly on the application, the oscillators must be exchangeable. The oscillators socket can hold DIL-8 or DIL-14 packages. Pin 1 is common for both types of packages.

3.3.2.1 VCXO with Feedback Loop

Oscillators of the VCXO type need a control signal at pin 1 (U_c). To get a closed feedback loop, this signal must be connected (via FPGA) to U_{out}. You have the possibility to build an RC loop filter be mounting R54, C41 and R53, C42. In this case, jumpers J30 and J31 remain open.

Crystal Oscillator	$U_{control}$ Signal	Clock source for
U3	XINIT	GCK0
U4	L43P	GCK1

Table 21: Crystal oscillator control signals and usage

Note: The jumper J31 (UC VCXO) must be inserted to connect pin 1 of U4 with signal *L43P* if a feedback signal for a VCXO is needed. Beware in mind that the *L43P* signals are connected in parallel if several boards are stacked. In this case, only U3 may be used in a PLL loop and J31 as well as the loop filter component R53 should be removed.

3.4 Reset and Voltage Supervision

U5 works as a reset and voltage supervision circuit. A functional reset can be issued at any time by pressing the push button SW2. The button is connected to the voltage supervisor circuit U5, which in turn generates a reset pulse on BUSY/DOUT (FPGA pin 178). A reset pulse is also generated whenever VCCINT drops below a predefined threshold of 2.2V (Spartan-II, Virtex) or 1.7V (Virtex-E) and on power up. The pulse duration is approximately 2ms. You can select the polarity of the reset pulse with jumper J23. The settings are listed in *Table 22*.

J23 (Reset)	Reset Pulse Polarity
1-2	Active Low
2-3	Active High

Table 22: Reset pulse polarity selection

Note: A manual reset initializes the internal circuits of the FPGA (registers, counters, finite state machines etc.) and must be implemented in the design appropriately. There is no dedicated reset pin on the FPGA.

3.5 User Buttons

Two user buttons (SW3 and SW4) are available for arbitrary purposes. A pressed button ties the connected FPGA pin to ground while the pin is pulled to VCCINT if the button is released.

Button	Signal Name	Spartan-II Pin	Virtex Pin
SW3	XWRITE	161	185
SW4	XCS	160	184

Table 23: User button connection with FPGA

The connection of a user button with the FPGA is routed over a 510Ω resistor. A pressed button does therefore not harm the SelectMAP interface.

3.6 LEDs

The eight LEDs D2 to D9 are intended as optical indicators for the display of status information. D1 is connected to the DONE pin of the FPGA and D10 (VCCOPT), D11 (VCCO) and D12 (VCCINT) serve as power indicator LEDs. The DONE LED turns on at the end of a successful bit stream download.

Note: The VCCO indicator LED D11 will not lit when the VCCO voltage is 1.5V or less since this value is below the forward voltage of the LED.

The LEDs D2 to D9 turn on whenever the corresponding FPGA output is low. Each LED may be disconnected from the I/O signal by removing the corresponding jumper. The following table shows the assignment to the jumpers and the FPGA pins:

LED	Jumper	Signal Name	Spartan-II Pin	Virtex Pin
D2	J14	L48P	46	56
D3	J13	L45N	57	67
D4	J12	L45P	58	68
D5	J11	L44P	60	71
D6	J10	L10N	168	195
D7	J9	L23N	132	152
D8	J8	L33N	100	113
D9	J7	L38N	84	96

Table 24: LED signals and corresponding FPGA pins

Note: If the board module is used within a stack the LEDs of all layers are connected in parallel. If a LED is driven by the FPGA the LEDs of the other layers are driven also. The maximal output current of 20mA of an FPGA port is sufficient for up to four layers. If more than four levels are used, or to avoid driving certain LEDs, the jumpers of the appropriate LEDs of the remaining layers must be removed.

3.7 Eight Position DIP Switch

The eight-position DIP switch SW1 can be used for application specific purposes. In the *On* position the connected FPGA pin is tied to ground. In the *Off* position the connected FPGA pin is pulled to VCCINT via a resistor.

The assignment of the switches to the FPGA pins is as follows:

Switch	Signal Name	Spartan-II Pin	Virtex Pin
1	D0/DIN	153	177
2	D1	146	167
3	D2	142	163
4	D3	135	156
5	D4	126	145
6	D5	119	138
7	D6	115	134
8	D7	108	124

Table 25: Signals on the eight position DIP switch

The switches are connected to the FPGA via resistors of 510Ω. Owing to these resistors, the SelectMAP mode can be used even if some switches are closed to ground.

3.8 Reference and I/O Signals

For the smaller FPGA devices some pins are usable as general I/Os whereas these pins are reference voltage inputs on the larger ones. Certain I/O standards need no reference voltages. In these cases, all of these pins may be used as general I/Os on every FPGA type.

To make the board as versatile as possible, you can connect every possible VREF pin individually to a reference voltage by inserting a jumper. *Table 26* gives an overview of the jumper groupings and assignments to the I/O banks. In *Table 27* the correspondence of each VREF jumper to the individual devices is listed. A jumper belongs to a certain device if there is a cross in the device column. No cross in the device column means that you can use the corresponding FPGA pin for general I/O.

Bank	Virtex and Spartan	Virtex only	Spartan only
7	J35, VREF_L61P J36, VREF_L57P J37, VREF_L60P	J39, VREF_7 J40, VREF10_7 J41, VREF610_7 J42, VREF_L63N	J38, L62N
6	J43, VREF_L50N J44, VREF_L51N	J45, VREF_L55P J46, VREF_L54N J47, VREF610_6 J48, VREF_6 J49, VREF10_6	J50, L54P J51, L49P
5	J52, VREF_L44N J53, VREF_L43N J54, VREF_L41P	J55, VREF_L46P J56, VREF_5 J57, VREF610_5 J58, VREF10_5	J59, L45N
4	J60, VREF_L34P J61, VREF_L35P	J62, VREF_L38P J63, VREF_L39N J64, VREF_4 J65, VREF10_4 J66, VREF610_4	J67, L38N J68, L33N
3	J69, VREF_L28N J70, VREF_L27N J71, VREF_L24N	J72, VREF_L30P J73, VREF_3 J74, VREF10_3 J75, VREF610_3	J76, L29N
2	J77, VREF_L21P J78, VREF_L18P J79, VREF_L17P	J80, VREF_L22N J81, VREF_2 J82, VREF10_2 J83, VREF610_2	J84, L16P
1	J85, VREF_L11P J86, VREF_L10P J87, VREF_L7P	J88, VREF_L13N J89, VREF_1 J90, VREF10_1 J91, VREF610_1	J92, L12P
0	J93, VREF_L2N J94, VREF_L0P	J95, VREF_L5N J96, VREF_0 J97, VREF40_0 J98, VREF610_0 J99, VREF610	J100, L5P J101, L1P

Table 26: Grouping, bank and signal assignment of VREF jumpers

Bank	Jumper and Signal	FPGA Device									
		XC2S50	XC2S100/150	XC2S200	XCV50E	XCV100E	XCV200E	XCV300E	XCV400E	XCV600E	XCV1000E
7	J35, VREF_L61P	X	X	X	X	X	X	X	X	X	X
	J36, VREF_L57P	X	X	X	X	X	X	X	X	X	X
	J37, VREF_L60P		X	X		X	X	X	X	X	X
	J38, L62N			X							
	J39, VREF_7								X	X	X
	J40, VREF10_7										X
	J41, VREF610_7									X	X
	J42, VREF_L63N					X	X	X	X	X	X
6	J43, VREF_L50N	X	X	X	X	X	X	X	X	X	X
	J44, VREF_L51N		X	X		X	X	X	X	X	X
	J45, VREF_L55P								X	X	X
	J46, VREF_L54N				X	X	X	X	X	X	X
	J47, VREF610_6									X	X
	J48, VREF_6					X	X	X	X	X	X
	J49, VREF10_6										X
	J50, L54P	X	X	X							
	J51, L49P			X							
5	J52, VREF_L44N	X	X	X	X	X	X	X	X	X	X
	J53, VREF_L43N		X	X		X	X	X	X	X	X
	J54, VREF_L41P	X	X	X	X	X	X	X	X	X	X
	J55, VREF_L46P						X	X	X	X	X
	J56, VREF_5								X	X	X
	J57, VREF610_5									X	X
	J58, VREF10_5										X
	J59, L45N			X							
4	J60, VREF_L34P	X	X	X	X	X	X	X	X	X	X
	J61, VREF_L35P		X	X		X	X	X	X	X	X
	J62, VREF_L38P				X	X	X	X	X	X	X
	J63, VREF_L39N								X	X	X
	J64, VREF_4						X	X	X	X	X
	J65, VREF10_4										X
	J66, VREF610_4									X	X
	J67, L38N	X	X	X							
	J68, L33N			X							

Bank	Jumper and Signal	FPGA Device									
		XC2S50	XC2S100/150	XC2S200	XCV50E	XCV100E	XCV200E	XCV300E	XCV400E	XCV600E	XCV1000E
3	J69, VREF_L28N	X	X	X	X	X	X	X	X	X	X
	J70, VREF_L27N		X	X		X	X	X	X	X	X
	J71, VREF_L24N	X	X	X	X	X	X	X	X	X	X
	J72, VREF_L30P						X	X	X	X	X
	J73, VREF_3								X	X	X
	J74, VREF10_3										X
	J75, VREF610_3									X	X
	J76, L29N			X							
2	J77, VREF_L21P	X	X	X	X	X	X	X	X	X	X
	J78, VREF_L18P		X	X		X	X	X	X	X	X
	J79, VREF_L17P	X	X	X	X	X	X	X	X	X	X
	J80, VREF_L22N								X	X	X
	J81, VREF_2						X	X	X	X	X
	J82, VREF10_2										X
	J83, VREF610_2									X	X
	J84, L16P			X							
1	J85, VREF_L11P	X	X	X	X	X	X	X	X	X	X
	J86, VREF_L10P					X	X	X	X	X	X
	J87, VREF_L7P	X	X	X	X	X	X	X	X	X	X
	J88, VREF_L13N						X	X	X	X	X
	J89, VREF_1								X	X	X
	J90, VREF10_1										X
	J91, VREF610_1									X	X
	J92, L12P			X							
0	J93, VREF_L2N		X	X		X	X	X	X	X	X
	J94, VREF_L0P	X	X	X			X	X	X	X	X
	J95, VREF_L5N				X	X	X	X	X	X	X
	J96, VREF_0				X	X	X	X	X	X	X
	J97, VREF40_0								X	X	X
	J98, VREF610_0									X	X
	J99, VREF610									X	X
	J100, L5P	X	X	X							
	J101, L1P			X							

Table 27: Correspondence of VREF jumpers to individual devices

3.9 ZBT RAM Option

The ZBT RAM U10 is an optional component of the module. If this RAM is present, the header connector ST5B, where all RAM signals are routed to, is not available. This is to avoid conflicts when you stack several boards.

The synchronous RAM clock input is specially handled. First, it may be driven directly from GCK2 over the coaxial SMB connector J17. In this case, you should use this GCK2 clock to drive the FPGA also. Doing the clocking that way, you have a true synchronous system clock for both FPGA and RAM. Second, you may drive the RAM clock from the FPGA output signal *L20N* (pin 138 on Spartan-II, pin 159 on Virtex-E) by inserting jumper J124. Now you are free to use any clock for the FPGA but the price to pay is that you do not have a true synchronous system clock for the RAM any more. However, you may use the DLLs of the FPGA to produce the system clock.

When you feed the clock from J17 (GCK2) you have the option to terminate the line with resistor R62 at the RAM, R51 at the FPGA or both.

You may put the RAM into *Linear Burst Mode* by inserting J122.

The following table summarizes what has been described above:

Option	Action to activate option
True synchronous clock for both FPGA and RAM	Feed external clock via J17 and remove jumper J124
FPGA output drives RAM clock, any clock drives FPGA	Insert jumper J124 and configure the FPGA to put out the RAM clock (on pin 138 for Spartan-II or pin 159 for Virtex-E)
Terminate GCK2 clock line at the FPGA	Solder R51 to the bottom of the board
Terminate the GCK2 clock line at the RAM	Solder R62 to the bottom of the board
Running RAM in linear burst mode	Insert jumper J122

Table 28: Options for running the RAM and their activation

3.10 Signals on Header Connectors

3.10.1 Signal Overview

All general I/O signals of the FPGA are routed to header connectors. This includes all the VREF pins also. If you want to operate a bank with an I/O standard that needs a reference voltage, you must connect all VREF pins of that bank to the appropriate reference voltage, see *3.8 Reference and I/O Signals*.

Note: When you stack several modules, the VREF signals of all modules are connected in parallel. Therefore you must use the same I/O standard for same banks on each module.

The tables on the following pages show the connections of the FPGA pins to the header connectors.

3.10.2 Signal Assignment to Connector ST4C

The following table shows the assignment of the FPGA pins to the ST4C connector pins:

Signal Name	Connector Pin	Spartan-II Pin	Virtex Pin	Signal Name	Connector Pin	Spartan-II Pin	Virtex Pin
VREF_L43N	101	62	73	VREF_L54N	126	-	36
VREF610_5	102	61	72	L54P	127	31	35
L44P	103	60	71	L55N	128	30	34
VREF_L44N	104	59	70	VREF_L55P	129	29	33
L45P	105	58	68	IO_6	130	27	31
L45N	106	57	67	L56N	131	24	28
VREF_L46P	107	-	66	L56P	132	23	27
L46N	108	-	65	VREF_7	133	22	26
L47P	109	-	64	L57N	134	21	24
L47N	110	-	63	VREF_L57P	135	20	23
L48N	111	-	57	L58N	136	18	21
L48P	112	46	56	L58P	137	17	20
VREF_6	113	49	54	VREF10_7	138	16	19
L49N	114	48	53	L59N	139	15	18
L49P	115	47	52	L59P	140	14	17
VREF_L50N	116	45	50	L60N	141	10	13
L50P	117	44	49	VREF_L60P	142	9	12
VREF610_6	118	43	48	VREF610_7	143	8	11
VREF_L51N	119	42	47	L61N	144	7	10
L51P	120	41	46	VREF_L61P	145	6	9
L52N	121	37	42	L62N	146	4	7
L52P	122	36	41	L62P	147	3	6
VREF10_6	123	35	40	VREF_L63N	148	-	5
L53N	124	34	39	L63P	149	5	4
L53P	125	33	38	IO_7	150	-	3

Table 29: Assignment of signals to the ST4C connector

3.10.3 Signal Assignment to Connector ST5A

The following table shows the assignment of the FPGA pins to the ST5A connector pins:

Signal Name	Connector Pin	Spartan-II Pin	Virtex Pin	Signal Name	Connector Pin	Spartan-II Pin	Virtex Pin
Unconnected	1	-	-	VREF_L22N	26	134	154
Button2	2	-	-	VREF_L21P	27	136	157
Button1	3	-	-	VREF10_2	28	140	161
VREF10_5	4	69	80	VREF_L18P	29	147	168
VREF_5	5	74	86	VRE610_2	30	148	169
VREF_L41P	6	73	84	VREF_L17P	31	-	171
DLL_L40N	7	-	87	VREF_2	32	-	175
VREF_L39N	8	82	94	L13P	33	-	186
VREF_L38P	9	-	97	VREF_L10P	34	167	194
L38N	10	84	96	VREF_L11P	35	164	191
VREF10_4	11	88	101	VREF610_1	36	166	193
VREF610_4	12	96	109	L10N	37	168	195
VREF_L35P	13	95	108	VREF10_1	38	174	201
VREF_L34P	14	98	111	L8P	39	175	202
L33N	15	100	113	VREF_L7P	40	178	205
VREF_4	16	102	115	VREF_1	41	180	208
L32P	17	-	118	VREF_0	42	202	231
VREF_L30P	18	-	126	VREF_L5N	43	-	218
VREF_L28N	19	111	130	L4P	44	191	220
VREF610_3	20	113	132	VREF610_0	45	193	222
VREF_L27N	21	114	133	VREF610	46	201	230
VREF10_3	22	121	140	VREF_L2N	47	200	229
VREF_L24N	23	125	144	VREF40_0	48	188	216
VREF_3	24	127	147	VREF_L0P	49	203	236
L23N	25	-	152	IO_0	50	-	238

Table 30: Assignment of signals to the ST5A connector

3.10.4 Signal Assignment to Connector ST5B

The following table shows the assignment of the FPGA pins to the ST5B connector pins. This connector is no present when the ZBT RAM is mounted on the board.

Signal Name	Connector Pin	Spartan-II Pin	Virtex Pin
Unconnected	51	-	-
L43P	52	63	74
L42N	53	67	78
L42P	54	68	79
IO_5	55	70	81
L41N	56	71	82
DLL_L40P	57	81	93
L39P	58	83	95
L37N	59	86	99
L37P	60	87	100
L36N	61	89	102
L36P	62	90	103
L35N	63	94	107
L34N	64	97	110
L33P	65	101	114
L32N	66	99	117
L30N	67	-	125
L29N	68	109	127
L29P	69	110	128
L28P	70	112	131
L26P	71	120	139
L25N	72	122	141
L25P	73	123	142
IO_3	74	129	149
L23P	75	133	153

Signal Name	Connector Pin	Spartan-II Pin	Virtex Pin
L22P	76	-	155
L20N	77	138	159
L20P	78	139	160
L19N	79	141	162
L17N	80	149	170
L16N	81	151	173
L16P	82	152	174
VREF_L13N	83	-	187
L12N	84	163	189
L12P	85	162	188
L11N	86	165	192
L9P	87	172	199
L9N	88	173	200
L8N	89	176	203
L7N	90	179	206
DLL_L6P	91	181	209
DLL_L6N	92	187	215
L5P	93	189	217
L4N	94	192	221
L3P	95	194	223
L3N	96	195	224
L2P	97	199	228
L1P	98	205	234
L1N	99	206	235
L0N	100	204	237

Table 31: Assignment of signals to the ST5B connector

3.10.5 Dedicated Signals

The header connector ST4B contains some dedicated signals which are used as clock and configuration signals. You can not change the function of these signals by any FPGA configuration.

Signal Name	ST4B Pin	Connected to Virtex pin
GCK0_ext	52	92 (over J26 1-2)
GCK1_ext	54	89 (over J27 1-2)
GCK2_ext	56	210 (over J28)
GCK3_ext	58	213 (over J29)
TCK	69	239
TMS	70	2
DUP	76	N/A (goes to pin 1 of J25)
DDOWN	77	N/A (goes to pin 4 of J25)

Table 32: Dedicated signals on connector ST4B

3.11 Stack Extension

When several board modules are stacked, the signal direction of I/O pins of different levels must be chosen very carefully. Short circuits between the FPGAs may result in damages or shortens their life. Not configured pins of the FPGA are in a high impedance state.

During the assembly of the stack you should pay attention to the fact that the pins of one module are aligned exactly with the holes of the sockets of the other module. A good possibility to accomplish this is the usage of two pieces of a prototyping board. Each of these pieces should have three rows with 50 holes. Before the assembly, these pieces are sled up to the ends of the connector pins. Thereby, the pin ends keep their positions.

To disassemble a stack we recommend the usage of pliers that are used to remove locking rings. The claws of the pliers should be covered with plastic or rubber tubes to prevent damages on the boards. The modules are then separated easily by repeated application of gentle pressure with the pliers on all four corners.

4 Literature

The following list is an excerpt from the Xilinx literature concerning the Virtex FPGA family. The corresponding PDF files may be downloaded directly from

http://www.xilinx.com/apps/virtexapp.htm
http://www.xilinx.com/apps/sp2app.htm

or be requested from a Xilinx distributor.

Application Notes

Virtex

- XAPP243: Bus LVDS with Virtex-E Devices
- XAPP242: Interfacing to Lara Networks Search Engine using Virtex Devices
- XAPP241: Virtex-EM FIR Filter for Video Applications
- XAPP240: High-Speed Buffered Crossbar Switch Design using Virtex-EM Devices
- XAPP237: Virtex-E LVPECL Receivers in Multi-Drop Applications
- XAPP235: Virtex-E Package Compatibility Guide
- XAPP234: Virtex SelectLink Communications Channel
- XAPP233: Multi-channel 622 Mb/s LVDS Data Transfer with Virtex-E Devices
- XAPP232: Virtex-E LVDS Drivers and Receivers: Interface Guidelines
- XAPP231: Multi-Drop LVDS with Virtex-E FPGAs
- XAPP230: The LVDS I/O Standard
- XAPP217: Gold Code Generators in Virtex Devices
- XAPP215: Design Tips for HDL Implementation of Arithmetic Functions
- XAPP214: Virtex Device Quad Data Rate (QDR) SRAM Interface
- XAPP212: CDMA Matched Filters Implementation in Virtex Devices
- XAPP211: PN Generators Using the Virtex SRL Macro
- XAPP210: Linear Feedback Shift Registers in Virtex Devices
- XAPP208: IDCT implementation in Virtex Devices for MPEG applications
- XAPP205: Data-Width Conversion FIFOs using Virtex Block SelectRAM Memory
- XAPP204: CAM in Block Select RAM
- XAPP203: Designing Flexible, Fast CAMs with Virtex Slices
- XAPP202: CAM in ATM applications
- XAPP201: An Overview of Multiple CAM Designs in Virtex Devices
- XAPP200: Double Data Rate SDRAM
- XAPP158: Powering Virtex FPGAs
- XAPP157: Board Routability Guidelines with Xilinx Fine-Pitch BGA Packages
- XAPP155: Virtex Analog to Digital Converter
- XAPP154: Virtex Synthesizable Delta-Sigma DAC

- XAPP153: Status and Control Semaphore Registers Using Partial Reconfiguration
- XAPP152: Virtex Power Estimator User Guide
- XAPP151: Virtex Configuration Architecture Advanced Users Guide
- XAPP137: Configuring Virtex FPGAs from Parallel EPROMs with a CPLD
- XAPP136: Synthesizable 143 MHz ZBT SRAM Interface
- XAPP135: Virtex I/V Curves for Various Output Options
- XAPP134: Virtex Synthesizable High Performance SDRAM Controller
- XAPP133: Using the Virtex SelectIO
- XAPP132: Using the Virtex Delay-Locked Loop
- XAPP131: 170MHz Synchronous and Asynchronous FIFOs Using the Virtex Block SelectRAM+
- XAPP130: Using the Virtex Block SelectRAM+

Spartan-II

- XAPP134: Synthesizable High Performance SDRAM Controller
- XAPP136: Synthesizable 200 MHz ZBT SRAM Interface
- XAPP142: Using Xilinx Programmable Logic with High-Speed Printers
- XAPP169: MP3 NG: A Next Generation Consumer Platform
- XAPP173: Using Block SelectRAM+ Memory in Spartan-II FPGAs
- XAPP174: Using Delay-Locked Loops in Spartan-II FPGAs
- XAPP175: High Speed FIFOs In Spartan-II FPGAs
- XAPP176: Spartan-II FPGA Family Configuration and Readback
- XAPP177: Spartan-II Family I/V Curves for Various Output Options
- XAPP178: Configuring Spartan-II FPGAs from Parallel EPROMs
- XAPP179: Using SelectI/O Interfaces in Spartan-II FPGAs
- XAPP200: Synthesizable 1.6 Gbytes/s DDR SDRAM Controller
- XAPP211: Pseudo-Random Noise Generators Using the SRL Macro

Data Book

- VirtexTM 2.5V Field Programmable Gate Arrays
- Virtex-E 1.8V Field Programmable Gate Arrays Datasheet
- Spartan-II Family FPGAs (XC2S00)

5 Appendix A: FPGA Pin Assignments

This appendix lists the FPGA pin assignments of devices compatible with the board module. The naming corresponds to the one in the Xilinx data sheet as far as possible.

- Active low signals are marked with a \ at the end of the name.
- For Spartan-II and Virtex devices, a general I/O signal is denoted with I/O.
- For Virtex-E devices, the signals are named with their low voltage differential input names.
- Dedicated signals and multipurpose signals (such which may change to general I/Os after configuration) are named with the function name they have prior to configuration.
- Reference voltage pins have the string VREF in their name.
- Shading indicates banking.

5.1 Special Considerations

1) Pins 25, 55, 85, 116, 146, 176, 207, 216 and 231 are I/O pins on Virtex devices whereas they are VCCO pins on Virtex-E devices. These pins are connected to VCCO on this board module. If you use this module with a Virtex device, configure these pins as input.
2) Pins 87 and 215 are VREF pins on Virtex devices whereas they are general I/Os on Virtex-E devices.
3) Pins 5, 12, 47, 73, 108, 133, 168, 194, and 229 are optional reference voltage pins in the Virtex 100E to 1000E devices.
4) Pins 54, 66, 115, 126, 175, 187 and 236 are optional reference voltage pins in the Virtex 200E to 1000E devices.
5) Pins 26, 33, 86, 94, 147, 154, 208 and 216 are optional reference voltage pins in the Virtex 400E to 1000E devices.
6) Pins 1, 48, 72, 109, 132, 169, 193, 222 and 230 are optional reference voltage pins in the Virtex 600E to 1000E devices.
7) Pins 19, 40, 80, 101, 140, 161 and 201 are optional reference voltage pins in the Virtex 1000E devices.

5.2 Spartan-II Devices in PQ-208 Package

Pin	Description
1	GND
2	TMS
3	I/O
4	I/O_VREF200
5	I/O
6	I/O_VREF
7	I/O
8	I/O
9	I/O_VREF100
10	I/O
11	GND
12	VCCO
13	VCCINT
14	I/O
15	I/O
16	I/O
17	I/O
18	I/O
19	GND
20	I/O
21	I/O_VREF
22	I/O
23	I/O
24	I/O_IRDY
25	GND
26	VCCO
27	I/O_TRDY
28	VCCINT
29	I/O
30	I/O
31	I/O_VREF
32	GND
33	I/O
34	I/O
35	I/O
36	I/O
37	I/O
38	VCCINT
39	VCCO
40	GND
41	I/O
42	I/O_VREF100
43	I/O
44	I/O
45	I/O_VREF
46	I/O
47	I/O_VREF200
48	I/O
49	I/O
50	M1
51	GND
52	M0
53	VCCO
54	M2
55	PWDN\
56	STATUS
57	I/O_VREF200
58	I/O
59	I/O_VREF
60	I/O
61	I/O
62	I/O_VREF100
63	I/O
64	GND
65	VCCO
66	VCCINT
67	I/O
68	I/O
69	I/O
70	I/O
71	I/O
72	GND
73	I/O_VREF
74	I/O
75	I/O
76	VCCINT
77	GCK1
78	VCCO
79	GND
80	GCK0
81	I/O
82	I/O
83	I/O
84	I/O_VREF
85	GND
86	I/O
87	I/O
88	I/O
89	I/O
90	I/O
91	VCCINT
92	VCCO
93	GND
94	I/O
95	I/O_VREF100
96	I/O
97	I/O
98	I/O_VREF
99	I/O
100	I/O_VREF200
101	I/O
102	I/O
103	GND
104	DONE
105	VCCO
106	PROGRAM\
107	I NIT\
108	D7
109	I/O_VREF200
110	I/O
111	I/O_VREF
112	I/O
113	I/O
114	I/O_VREF100
115	D6
116	GND
117	VCCO
118	VCCINT
119	D5

120	I/O
121	I/O
122	I/O
123	I/O
124	GND
125	I/O_VREF
126	D4
127	I/O
128	VCCINT
129	I/O_TRDY
130	VCCO
131	GND
132	I/O_IRDY
133	I/O
134	I/O
135	D3
136	I/O_VREF
137	GND
138	I/O
139	I/O
140	I/O
141	I/O
142	D2
143	VCCINT
144	VCCO
145	GND
146	D1
147	I/O_VREF100
148	I/O
149	I/O
150	I/O_VREF
151	I/O
152	I/O_VREF200
153	D0/DIN
154	BUSY/DOUT
155	CCLK
156	VCCO
157	TDO
158	GND
159	TDI
160	CS\
161	WR\
162	I/O_VREF200
163	I/O
164	I/O_VREF
165	I/O
166	I/O
167	I/O_VREF100
168	I/O
169	GND
170	VCCO
171	VCCINT
172	I/O
173	I/O
174	I/O
175	I/O
176	I/O
177	GND
178	I/O_VREF
179	I/O
180	I/O
181	I/O
182	GCK2
183	GND
184	VCCO
185	GCK3
186	VCCINT
187	I/O
188	I/O
189	I/O_VREF
190	GND
191	I/O
192	I/O
193	I/O
194	I/O
195	I/O
196	VCCINT
197	VCCO
198	GND
199	I/O
200	I/O_VREF100
201	I/O
202	I/O
203	I/O_VREF
204	I/O
205	I/O_VREF200
206	I/O
207	TCK
208	VCCO

Table 33: Pin assignment of Spartan-II FPGAs in the PQ-208 package

- Pins denoted with I/O_VREF are optional reference voltage pins on all devices.
- Pins denoted with I/O_VREF100 are additional reference voltage pins on XC2S100 and XC2S150 devices.
- Pins denoted with I/O_VREF200 are additional reference voltage pins on XC2S200 devices.

5.3 Virtex Devices in HQ-240 Package

Pin	Description
1	GND
2	TMS
3	I/O
4	I/O
5	VREF7
6	I/O
7	I/O
8	GND
9	VREF7
10	I/O
11	VREF7
12	VREF7
13	I/O
14	GND
15	VCCO
16	VCCINT
17	I/O
18	I/O
19	VREF7
20	I/O
21	I/O
22	GND
23	VREF7
24	I/O
25	I/O
26	VREF7
27	I/O
28	I/O
29	GND
30	VCCO
31	I/O
32	VCCINT
33	VREF6
34	I/O
35	I/O
36	VREF6
37	GND
38	I/O
39	I/O
40	VREF6
41	I/O
42	I/O
43	VCCINT
44	VCCO
45	GND
46	I/O
47	VREF6
48	VREF6
49	I/O
50	VREF6
51	GND
52	I/O
53	I/O
54	VREF6
55	I/O
56	I/O
57	I/O
58	M1
59	GND
60	M0
61	VCCO
62	M2
63	I/O
64	I/O
65	I/O
66	VREF5
67	I/O
68	I/O
69	GND
70	VREF5
71	I/O
72	VREF5
73	VREF5
74	I/O
75	GND
76	VCCO
77	VCCINT
78	I/O
79	I/O
80	VREF5
81	I/O
82	I/O
83	GND
84	VREF5
85	I/O
86	I/O
87	VREF5
88	VCCINT
89	GCK1
90	VCCO
91	GND
92	GCK0
93	I/O
94	VREF4
95	I/O
96	I/O
97	VREF4
98	GND
99	I/O
100	I/O
101	VREF4
102	I/O
103	I/O
104	VCCINT
105	VCCO
106	GND
107	I/O
108	VREF4
109	VREF4
110	I/O
111	VREF4
112	GND
113	I/O
114	I/O
115	VREF4
116	I/O
117	I/O
118	I/O
119	GND

120	DONE
121	VCCO
122	PROGRAM\
123	INIT\
124	D7
125	I/O
126	VREF3
127	I/O
128	I/O
129	GND
130	VREF3
131	I/O
132	VREF3
133	VREF3
134	D6
135	GND
136	VCCO
137	VCCINT
138	D5
139	I/O
140	VREF3
141	I/O
142	I/O
143	GND
144	VREF3
145	D4
146	I/O
147	VREF3
148	VCCINT
149	I/O
150	VCCO
151	GND
152	I/O
153	I/O
154	VREF2
155	I/O
156	D3
157	VREF2
158	GND
159	I/O
160	I/O
161	VREF2
162	I/O
163	D2
164	VCCINT
165	VCCO
166	GND
167	D1
168	VREF2
169	VREF2
170	I/O
171	VREF2
172	GND
173	I/O
174	I/O
175	VREF2
176	I/O
177	D0/DIN
178	BUSY/DOUT
179	CCLK
180	VCCO
181	TDO
182	GND
183	TDI
184	CS\
185	WRITE\
186	I/O
187	VREF1
188	I/O
189	I/O
190	GND
191	VREF1
192	I/O
193	VREF1
194	VREF1
195	I/O
196	GND
197	VCCO
198	VCCINT
199	I/O
200	I/O
201	VREF1
202	I/O
203	I/O
204	GND
205	VREF1
206	I/O
207	I/O
208	VREF1
209	I/O
210	GCK2
211	GND
212	VCCO
213	GCK3
214	VCCINT
215	VREF0
216	I/O
217	I/O
218	VREF0
219	GND
220	I/O
221	I/O
222	VREF0
223	I/O
224	I/O
225	VCCINT
226	VCCO
227	GND
228	I/O
229	VREF0
230	VREF0
231	I/O
232	VREF0
233	GND
234	I/O
235	I/O
236	VREF0
237	I/O
238	I/O
239	TCK
240	VCCO

Table 34: Pin assignment of Virtex FPGAs in the HQ-240 package

5.4 Virtex-E Devices in HQ-240 Package

Pin	Description
1	GND
2	TMS
3	IO_7
4	L63P
5	VREF_L63N
6	L62P
7	L62N
8	GND
9	VREF_L61P
10	L61N
11	VREF610_7
12	VREF_L60P
13	L60N
14	GND
15	VCCO
16	VCCINT
17	L59P
18	L59N
19	VREF10_7
20	L58P
21	L58N
22	GND
23	VREF_L57P
24	L57N
25	VCCO
26	VREF_7
27	L56P
28	L56N
29	GND
30	VCCO
31	IO_6
32	VCCINT
33	VREF_L55P
34	L55N
35	L54P
36	VREF_L54N
37	GND
38	L53P
39	L53N
40	VREF10_6
41	L52P
42	L52N
43	VCCINT
44	VCCO
45	GND
46	L51P
47	VREF_L51N
48	VREF610_6
49	L50P
50	VREF_L50N
51	GND
52	L49P
53	L49N
54	VREF_6
55	VCCO
56	L48P
57	L48N
58	M1
59	GND
60	M0
61	VCCO
62	M2
63	L47N
64	L47P
65	L46N
66	VREF_L46P
67	L45N
68	L45P
69	GND
70	VREF_L44N
71	L44P
72	VREF610_5
73	VREF_L43N
74	L43P
75	GND
76	VCCO
77	VCCINT
78	L42N
79	L42P
80	VREF10_5
81	IO_5
82	L41N
83	GND
84	VREF_L41P
85	VCCO
86	VREF_5
87	DLL_L40N
88	VCCINT
89	GCK1
90	VCCO
91	GND
92	GCK0
93	IDLL_L40P
94	VREF_L39N
95	L39P
96	L38N
97	VREF_L38P
98	GND
99	L37N
100	L37P
101	VREF10_4
102	L36N
103	L36P
104	VCCINT
105	VCCO
106	GND
107	L35N
108	VREF_L35P
109	VREF610_4
110	L34N
111	VREF_L34P
112	GND
113	L33N
114	L33P
115	VREF_4
116	VCCO
117	L32N
118	L32P
119	GND

120	DONE
121	VCCO
122	PROGRAM\
123	INIT\
124	D7
125	L30N
126	VREF_L30P
127	L29N
128	L29P
129	GND
130	VREF_L28N
131	L28P
132	VREF610_3
133	VREF_L27N
134	D6
135	GND
136	VCCO
137	VCCINT
138	D5
139	L26P
140	VREF10_3
141	L25N
142	L25P
143	GND
144	VREF_L24N
145	D4
146	VCCO
147	VREF_3
148	VCCINT
149	IO_3
150	VCCO
151	GND
152	L23N
153	L23P
154	VREF_L22N
155	L22P
156	D3
157	VREF_L21P
158	GND
159	L20N
160	L20P
161	VREF10_2
162	L19N
163	D2
164	VCCINT
165	VCCO
166	GND
167	D1
168	VREF_L18P
169	VREF610_2
170	L17N
171	VREF_L17P
172	GND
173	L16N
174	L16P
175	VREF_2
176	VCCO
177	D0/DIN
178	BUSY/DOUT
179	CCLK
180	VCCO
181	TDO
182	GND
183	TDI
184	CS\
185	WRITE\
186	L13P
187	VREF_L13N
188	L12P
189	L12N
190	GND
191	VREFL11P
192	L11N
193	VREF610_1
194	VREF_L10P
195	L10N
196	GND
197	VCCO
198	VCCINT
199	L9P
200	L9N
201	VREF10_1
202	L8P
203	L8N
204	GND
205	VREF_L7P
206	L7N
207	VCCO
208	VREF_1
209	DLL_L6P
210	GCK2
211	GND
212	VCCO
213	GCK3
214	VCCINT
215	DLL_L6N
216	VREF_0
217	L5P
218	VREF_L5N
219	GND
220	L4P
221	L4N
222	VREF610_0
223	L3P
224	L3N
225	VCCINT
226	VCCO
227	GND
228	L2P
229	VREF_L2N
230	VREF610
231	VREF40_0
232	VCCO
233	GND
234	L1P
235	L1N
236	VREF_L0P
237	L0N
238	IO_0
239	TCK
240	VCCO

Table 35: Pin assignment of Virtex-E FPGAs in the HQ-240 package

6 Appendix B: Changes and Improvements

This appendix lists the changes and improvements of the board module compared to its predecessor EVALXCV-HQ240.

Changes

- The signals TDI and TDO are no longer routed to the pins 68 and 71 of ST4B. This makes it now possible to interconnect stacked boards in a single JTAG chain.
- Connectors J4 (XChecker) and J5 (JTAG) now have two rows to enable the wiring of external configuration chains within a stack.
- The order of the power connectors for VCCINT, VCCO and VCCOPT is now the same as on the power module PWR3.

Additional Features

- User buttons are now also accessible on header connector ST5A at pin 2 (Button 2) and pin 3 (Button3). When you stack several boards, the buttons will now be connected in parallel. Pressing the button of the topmost board has now the same effect as pressing the same button on all boards simultaneously. We have done this because it is not possible to reach either button 1 or button 2 with a finger when the boards are stacked.
- A synchronous ZBT RAM has been added. It gets its clock either from GCK2 (synchronous clock for both FPGA and RAM) or from an output of the FPGA.

7 Appendix C: Schematic Diagram and PCB Layout

The following pages show the technical details of the board:

- Top overlay silk screen and top layer
- Mid layer 1
- Mid layer 2
- Bottom overlay silk screen and bottom layer
- Schematic diagram

The ground plane and the supply voltage plane are not shown.