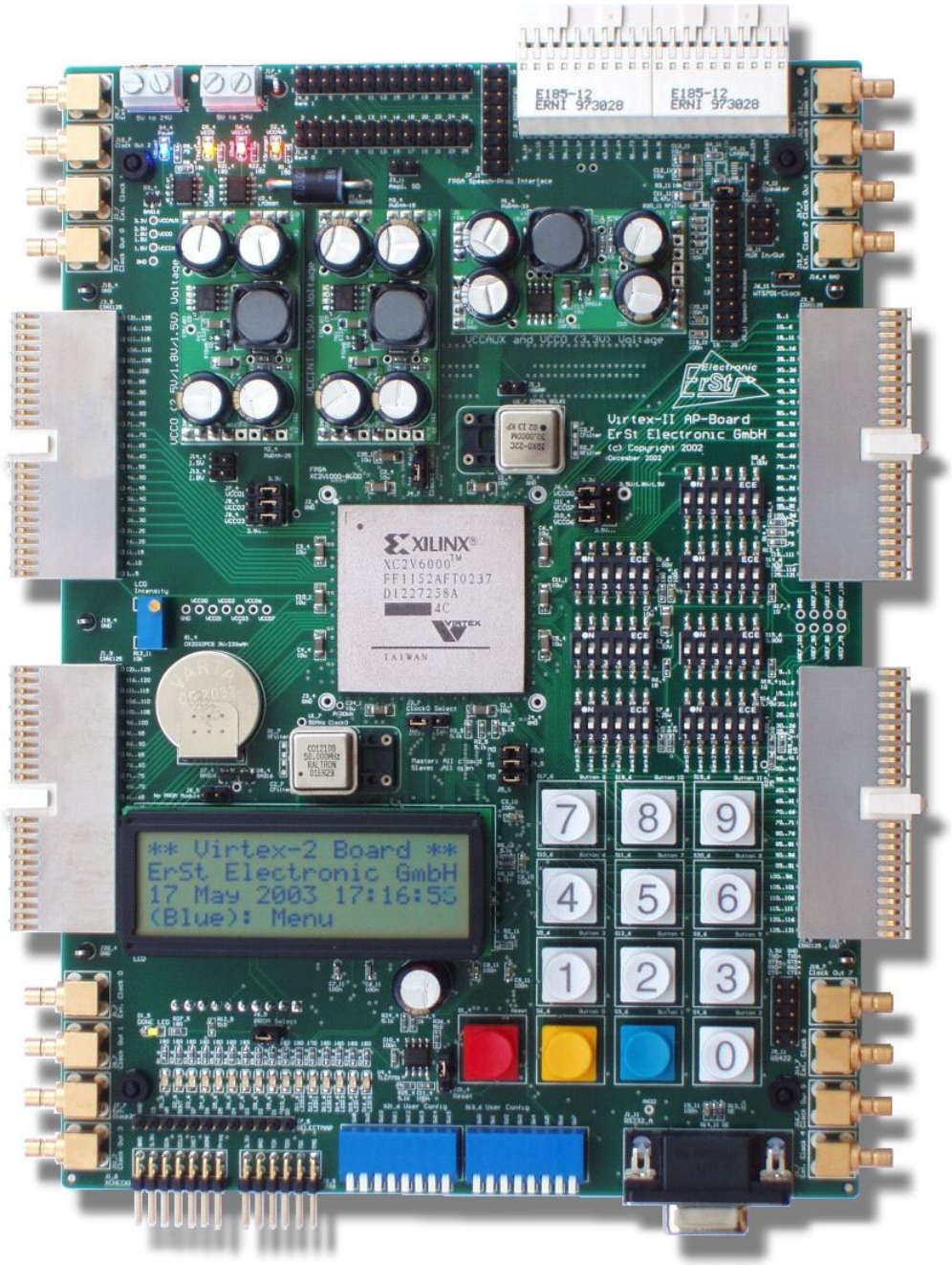
Virtex-II

Prototyping Board

User Manual



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Manual Version: Virtex-II Version 1.2 June 2003

This manual describes the technical properties and the usage of the following products:

Virtex-II Prototyping Board: Version 1.0 February 2003

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Notational Conventions

1. Names of active low signals are marked with a trailing \ or start with x, e.g. CS\ or XCS.
2. When used to describe signal voltage levels, 0 means low voltage, 1 means high voltage.
3. Table and figure references are printed in an italic font.
4. Signal names within a sentence are printed in an italic font.

Background Colors

The following background colors are used in the pin tables to mark pins that are not available on certain devices or have additional special functions:

(1) Pins are not available on the XC2V1000

(3) Pins are not available on the XC2V3000

(1), (5) Pins are not available on the XC2V1000 and XC2V1500

(TTSP) Pins marked with (TTSP) also connect to the text-to-speech processor if the jumpers J3_11 and J7_11 are inserted

(LCD) Pins marked with (LCD) are also connected with the LCD module, see paragraph 5.12

Abbreviations

ASIC	Application Specific Integrated Circuit
BGA	Ball Grid Array
DC	Direct Current
DCI	Digitally Controlled Impedance
DES	Data Encryption Standard
DIL	Dual Inline
DIP	Dual Inline Package
DLL	Delay-Locked Loop
DPR	Dual Port RAM
ESD	Electrostatic Discharge
FF896	Fine pitch Flip-chip BGA package with 896 balls
FF1152	Fine pitch Flip-chip BGA package with 1152 balls
FPGA	Field Programmable Gate Array
GND	System Ground
HQ	Thermally enhanced QFP
IEEE	Institute of Electrical and Electronics Engineers
IOB	Input / Output Block
IP	Intellectual Property
ISP	In System Programmable
JTAG	Joint Test Action Group
LCD	Liquid Crystal Display
LED	Light Emitting Diode
LVDS	Low Voltage Differential Signal
OTP	One Time Programmable
PC	Personal Computer
PCB	Printed Circuit Board
PLCC	Plastic Leaded Chip Carrier
PLL	Phase Locked Loop
PROM	Programmable Read Only Memory
PWM	Pulse Width Modulation
QFP	Quad Flat Pack
RAM	Random Access Memory
RTC	Real Time Clock
SCP	Serial Configuration PROM
SMD	Surface Mounted Device
SPI	Serial Peripheral Interface
SPROM	Serial PROM
SRAM	Static RAM
TTSP	Text-To-Speech Processor
UART	Universal Asynchronous Receiver & Transmitter
VCCINT	Internal supply voltage
VCCO	Output driver supply voltage
VCCOPT	Optional supply voltage
VCXO	Voltage Controlled Crystal Oscillator
VQ	Plastic very thin QFP
ZBT	Zero Bus Time

Virtex-II is a trademark of Xilinx Inc.

Revision History

Date	Version	Description
February 28, 2003	1.0	Initial release
April 22, 2003	1.1	Pin number assignments updated/corrected Pin table background colors introduced
June 23, 2003	1.2	Error in pin tables corrected, new title page image

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1 Introduction

This manual describes the specific properties of the prototyping board like power supply, reference voltages, FPGA configuration, clocks, reset, LEDs, DIP-switches, LCD, text-to-speech processor, RS-232/422 interface, RAMs and I/O signals.

Please take information about the FPGA from the Xilinx literature (see *Appendix B: Literature*). Online information can be found on the Xilinx websites:

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Chapter 2 lists the key features of the prototyping board.

Chapter 3 gives an overview of the prototyping board. The key features are listed and some application ideas are given. A introductory function description of the building blocks is given.

Chapter 4 is for the first time user. The factory settings (shipping state) are described here. There is also a short description about the board configuration with user supplied bit streams using JTAG and XChecker download methods.

Chapter 5 contains all the technical information and details of the board. All building blocks are covered here in details. Most of the relevant information like jumper settings and signals assignments is presented as tables.

Chapter 6 contains detailed tables of all external connector pin assignments to the FPGA I/O pins.

Chapter 7 lists some available Xilinx application notes and other Virtex-II related literature.

Chapter 8 shows the detailed PCB layouts, mechanical drawings and schematic diagrams.

2 Key Features

Mainboard
- One Virtex-II FPGA in the FF1152 package
- Board size 211.5mm x 150mm
- Several boards may be connected to form a stack

Clock
- Two separate crystal oscillators with sockets (DIL8 or DIL14)
- Jumpers to select between internal and external clock sources
- 16 SMB coaxial connectors for input and output of high frequency clocks

General I/Os
- Four banks routed directly to ERmet® 2mm Hard Metric connectors complying to the international standard IEC 61076-4-101
- One differential signal connector with 60 LVDS pairs

Power Supply
- Three DC/DC converters for internal, auxiliary and output supplies
- Board can be operated from a single 5V to 24V supply
- I/O bank reference voltages: VREFs of six banks individually selectable with DIP-switches from a total of seven predefined reference voltages
- Battery backed up real time clock (RTC)
- Voltage supervisor with reset button

Memory
- Fast static RAM 2x256KBx16, 12ns
- Optional dual port RAM (2x128KBx8)

User Interface
- Twelve general purpose push buttons
- One dedicated push button for reset pulse generation
- Two eight position DIP switches
- Display with sixteen LEDs
- Liquid Crystal Display with green-yellow back light and 4 lines with 20 characters
- Text-to-speech processor with audio power amplifier, accepts ASCII input via a SPI port and converts it to spoken audio
- "Done" LED to show successful bit stream download
- Power LEDs for input power and DC/DC converter outputs
- RS-232 Line driver/receiver, DB-9 female connector
- RS-422 Line driver/receiver

Configuration
- Mode jumpers M0 / M1 / M2
- Download: Master Serial Mode from ISP SPROM, Slave Serial Mode (XChecker header connector), Boundary Scan Mode (JTAG header connector), SelectMAP Mode (header connector)
- Configuration from onboard SCPs: ISP SCPs programmable via JTAG

Applications
- Implementation of custom designs using the full power of the Virtex-II architecture
- Evaluate Virtex-II FPGA families in the FF1152 package
- Quickly and easily expand the complexity of the system by stacking several boards and using partitioning software
- Tests of algorithms under real time conditions and watch the signals with a logic analyzer
- Experiment with different low voltage I/O standards and differential signals
- ASIC Emulation
- Error monitoring and analysis
- Digital PLL circuits
- PWM controller
- Adaptive digital filters
- Signal multiplexers
- Stimuli generators
- High speed encoder/decoder
- Memory controller
- Interface controller

This board provides all the necessary basic components needed in most of FPGA-based designs. Special care has been dedicated to routing topology and signal integrity. Most of the I/Os are routed to ERmet® 2mm Hard Metric connectors complying to the international standard IEC 61076-4-101. By combining two or more Virtex-II boards and using partitioning software you can easily distribute your design over several FPGAs to cope with complex designs that exceed the scope of a single FPGA.

The Virtex-II development board gives you an ideal platform for evaluating, implementing, testing, and extending custom designs using Virtex-II devices. You can also easily integrate the board into a larger system. The board is equipped with onboard power supplies and can be operated from a single 5V to 24V power supply. This makes it great for teaching, seminars, and courses.

3 Function Description

The Virtex-II prototyping module contains a Xilinx Virtex-II FPGA in the FF1152 package. This board is especially suited to test digital circuits during the early stages of their development. You can easily attach a logic analyzer and watch the signals in real time. The high count of system gates enables you to implement circuits that reach the complexity of ASICs. The configuration data of the FPGA is downloadable using one of four modes (master serial mode (XChecker), slave serial mode (SPROM), boundary scan ode (JTAG) and SelectMAP mode). The block diagram of *Figure 1: Block diagram of the prototyping board* shows the functional blocks of the board.

Six banks of general I/Os of the FPGA are routed to ERmet® 2mm Hard Metric connectors, four connectors for ground based signals and one differential signal connector. If you use I/O standards that need reference voltages, you can select up to seven different voltage levels for all six banks individually with DIP-switches.

A fast asynchronous static RAM and an optional dual port RAM help you to support memory demanding implementations like imaging and telecommunication applications.

By connecting several boards you may implement circuits whose complexity is beyond the scope of a single FPGA. The whole stack is configurable with a single download by externally daisy chaining the JTAG chain. To facilitate the connection of external hardware or further Virtex-II boards, we created various ties and adapters for both single and differential signals. The ties provide point to point connections between Virtex-II boards with the possibility to connect oscilloscopes and logic analyzers, whereas the adapters enable you to connect ribbon cables to standard 0.1” header connectors.

A ISP SCP (XC18V04 family) module is pluggable to the board. You can program these SCPs using the JTAG mode.

A total of 16 clock sources can be connected using coaxial SMB connectors. Two clocks are either an onboard crystal oscillator or an external source. The other sources are always external sources. It is also possible to output a clock from the FPGA via these connectors.

The crystal oscillators are housed in standard DIL-8 or DIL-14 size metal cans plugged into sockets, so you can easily change the frequency.

A voltage supervisor circuit generates a short pulse of ca. 2ms duration whenever the core supply voltage (VCCINT) drops below 1.3V and on power up. Such a reset pulse is also generated when you press the reset button.

A real time clock (RTC) with lithium battery is available for applications that need date/time information. The battery also keeps the DES key RAM of the FPGA from loosing its contents.

A 9 pole female D-Sub connector and a transceiver device provide a mean to connect serial devices like a PC to the prototyping board. The transceiver performs the voltage level translation and ESD protection of the RxD and TxD lines. The UART functionality must be implemented in the FPGA. Differential line drivers (RS-422) may be used instead of the RS-232 drivers to achieve bit rates in excess of 10Mb/s.

Push buttons, DIP-switches, LEDs and an LCD form a user interface that allows you to provide configuration data and monitor status information from the running system.

Two eight-position DIP switches are available for user specific applications. Twelve push buttons form a key-pad and can be used to input user data. One push button is connected to the voltage supervisor which generates a short pulse when this button is pressed.

A row with 16 LEDs may function as a display for status and error messages.

A liquid crystal display with 4 lines with 20 character, green-yellow back light and parallel interface provides an advanced mean for displaying more detailed debugging information during development.

A text-to-speech processor and an audio power amplifier form a text-to-speech unit that accepts ASCII input via a SPI port and converts it to spoken audio.

Three DC/DC converters generate all necessary low voltages from a single 5V to 24V input. Seven reference voltages are derived from the 3.3V converter.

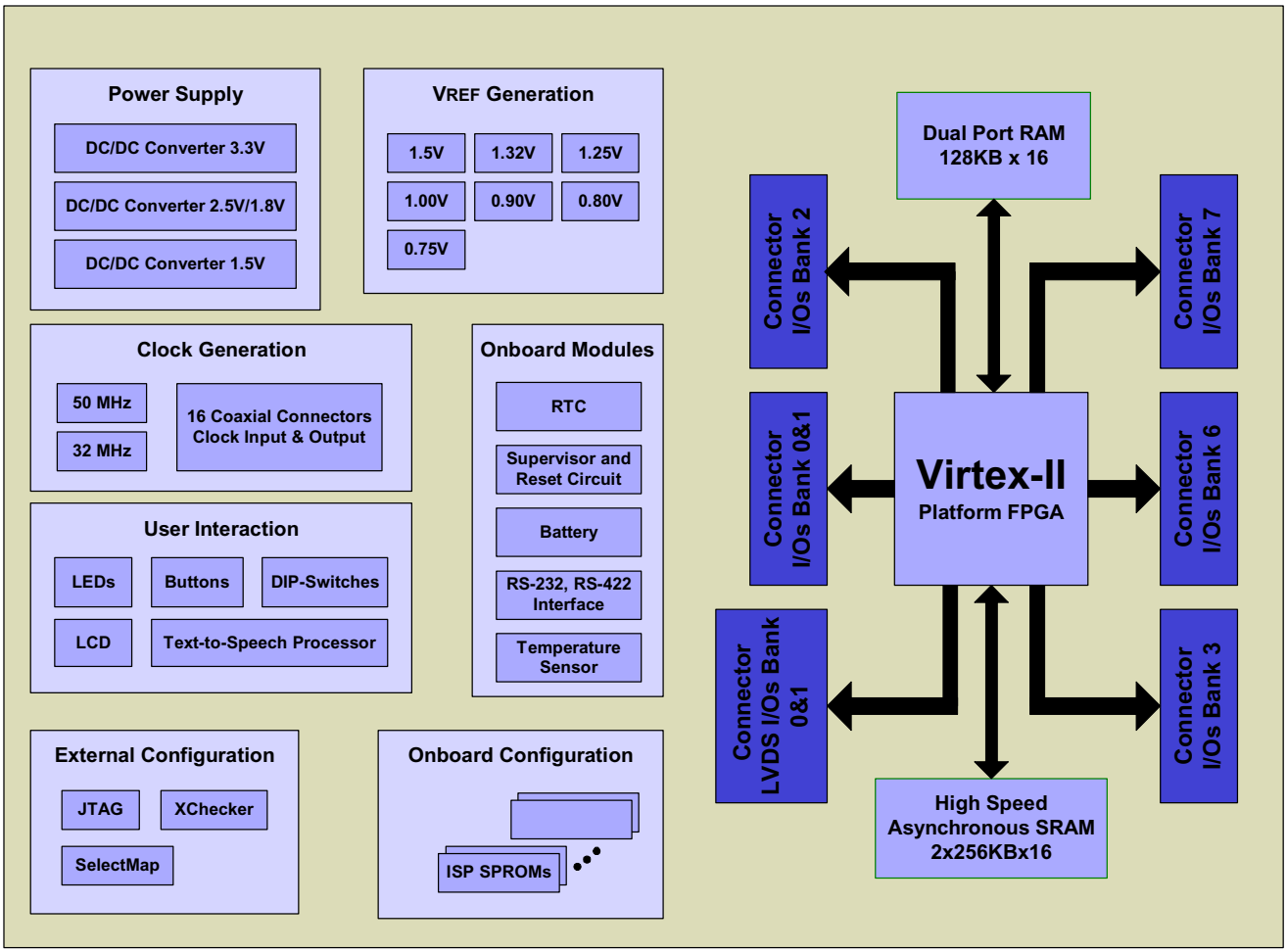

Figure 1: Block diagram of the prototyping board.

4 Getting Started

4.1 Factory Settings

Upon delivery of the Virtex-II prototyping board, the SPROM module contains a test code that is loaded into the FPGA on power up. All jumpers are set correctly for this configuration. To verify the correct operation of the board you should do the following steps:

1) Apply power (5V to 24V) on the power input connector J1_4: The power LEDs should turn on immediately and the DONE LED should turn on after a short delay.

2) The FPGA is now configured and starts to execute several tasks:
   - The user LEDs flash randomly, one or more at the same time with pauses of random duration.
   - The text-to-speech processor narrates a welcome message. Pressing a number key or the yellow or blue key also generates a spoken response.
   - The LCD provides a menu that allows you to set/display the time/date and to measure the ambient temperature and the temperature of the FPGA.

3) The left DIP-switch block (the one next to the JTAG configuration connector) allows for the following configuration:
   - **Switch 1:** Assignment of LCD. The LCD is assigned to time/date and temperature function if this switch is in the OFF position. When the switch is in the ON position, the LCD is assigned to the text-to-speech processor.
   - **Switch 6-8:** Volume control of TTSP. Maximum volume is configured when all three switches are in the OFF position. Minimum volume is configured if all three switches are in the ON position. Other combinations specify intermediate binary coded values.

4) The FPGA operation can be interrupted and restarted by pressing the (red) reset button.

4.2 JTAG Programming

JTAG programming is the most commonly used method to download a bit stream into the FPGA or program the SPROMs. This mode can always be used and needs no special mode selections. We assume that you are familiar with the download software and describe here only the steps that are special for this board.

Do the following steps to download a bit stream to the FPGA:

1) Apply power to the board.

2) Connect the download cable to the JTAG connector according to *Table 8: JTAG port pin assignment.*

3) Start downloading software. If you are downloading to this board for the first time, you have to set up the JTAG chain first. *See Table 7: ISP SPROM module composition and JTAG chains* for a description of the possible configurations. Many download programs are able to identify the proper chain automatically without the need to specify the chain explicitly.

4) You can now download the bit stream to the FPGA directly or program the PROM module.

Note: *Although the direct configuration of the FPGA and the PROM programming is done via the JTAG interface, the involved bit streams are not identical!*

For the direct configuration you need to set JTAG clock in the bit stream generator whereas you have to set the CCLK option when generating a bit stream for PROM programming. That is because the PROMs will be read out from the FPGA in master serial mode where the FPGA generates the CCLK.

4.3 XChecker Programming

This method works with the slave serial mode where the programmer software generates the clock signal.

Do the following steps to download a bit stream to the FPGA:

1) Remove jumpers J3_5, J4_5 and J5_5 to select slave serial mode.

2) Remove J6_5 to deselect the onboard SPROM module.

3) Apply power to the board.

4) Connect the download cable to the XChecker connector according to *Table 11: XChecker port pin assignment.*

5) Start the downloading software and download the bit stream to the FPGA. Do remember to set the CCLK option in the bit stream generator, see previous note.

5 Technical Information

This chapter gives a detailed description of the technical details of the board. Please consult the schematic diagrams where you find the components whose designators are mentioned in the text.

5.1 Power Supply

Due to the 0.13µm process, the FPGA works with an internal supply voltage (VCCINT) of 1.5V and an output driver voltage (VCCO) of up to max. 3.3V. Depending on the chosen I/O standard, VCCO can be 1.5V, 1.8V, 2.5V or 3.3V. The inputs are 5V tolerant only in combination with a series resistor of at least 100 Ω. Other devices on the board need a supply voltage of 3.3V. This voltage is derived from the 3.3V DC/DC converter that also supplies the VCCAUX voltage. Internal supply and output driver voltages are also generated with DC/DC converters. All three DC/DC converters (VCCINT, VCCO and VCCAUX) operate from a single 5V to 24V external power and are capable to produce an output current in excess of 4A.

Input power is fed through connector J1_4 or J12_4. The diode D1_4 protects the board from an accidentally applied reverse voltage.

5.1.1 3.3V (VCCAUX) Supply

A 3.3V supply (generated by module M1_4) is needed for various devices (SPROMs, crystal oscillators, voltage supervisor, general purpose LEDs, LCD, text-to-speech processor, audio amplifier, temperature sensor, RTC, RS-232/422 drivers, JTAG and XChecker ports). It is also the VCCAUX supply of the FPGA. In the case of a VCCO voltage of 3.3V, this supply is also used for VCCO.

5.1.2 1.5V to 2.5V (VCCO) Supply

This supply is generated by module M2_4. It is exclusively used for VCCO and its voltage can be set to 1.5V, 1.8V or 2.5V according to the following table:

VCCO Voltage	Jumper Setting
1.5V	J14_4 inserted
1.8V	J13_4 inserted
2.5V	No jumper inserted

Table 1: Jumper settings for VCCO voltage selection.

5.1.3 1.5V (VCCINT) Supply

This supply (M3_4) is exclusively used for VCCINT of the FPGA, its voltage is fixed to 1.5V.

5.1.4 Output Driver Supply Voltage

You can connect each of the six I/O bank's (bank 0,1,2,3,6 and 7) output driver supply to the VCCO voltage individually. To do this, set the jumpers according to the following table:

Bank	3.3V from M1_4	2.5V, 1.8V or 1.5V from M2_4
0	J6_4(1-2)	J6_4(2-3)
1	J7_4(1-2)	J7_4(2-3)
2	J8_4(1-2)	J8_4(2-3)
3	J9_4(1-2)	J9_4(2-3)
6	J10_4(1-2)	J10_4(2-3)
7	J11_4(1-2)	J11_4(2-3)

Table 2: Selecting the output driver voltage.

The VCCO voltage comes from the power module M1_4 (3.3V) or M2_4 (1.5V to 2.5V) and can be selected to be 1.5V, 1,8V, 2.5V or 3.3V. If you use an I/O standard that does not require an output driver voltage, just remove the corresponding jumper. If you need two or three different output driver voltages in the range 1.5V to 2.5V at the same time, you can do this be removing the appropriate jumper and using the center pin (pin 2) to connect an external supply.

5.1.5 Reference Voltages

The FPGA has six I/O banks that can be supplied with different reference voltages depending on the used I/O standard. For your convenience, all reference voltages are generated on the board, derived from 3.3V using a resistor network for voltage division. These internal reference voltages can be monitored at test points.

The choice of a dedicated reference voltage source for each bank is made by properly setting DIP-switches according to the following table:

Bank	VREF	DIP-Switch Settings						
		S1_6	S2_6	S7_6	S8_6	S14_6	S15_6	S16_6
0	0.75V							On(1)
0	0.80V						On(1)	
0	0.90V					On(1)		
0	1.00V				On(1)			
0	1.25V			On(1)				
0	1.32V		On(1)					
0	1.50V	On(1)						

Bank	VREF	DIP-Switch Settings						
		S1_6	S2_6	S7_6	S8_6	S14_6	S15_6	S16_6
1	0.75V							On(2)
1	0.80V						On(2)	
1	0.90V					On(2)		
1	1.00V				On(2)			
1	1.25V			On(2)				
1	1.32V		On(2)					
1	1.50V	On(2)						
2	0.75V							On(3)
2	0.80V						On(3)	
2	0.90V					On(3)		
2	1.00V				On(3)			
2	1.25V			On(3)				
2	1.32V		On(3)					
2	1.50V	On(3)						
3	0.75V							On(4)
3	0.80V						On(4)	
3	0.90V					On(4)		
3	1.00V				On(4)			
3	1.25V			On(4)				
3	1.32V		On(4)					
3	1.50V	On(4)						
6	0.75V							On(5)
6	0.80V						On(5)	
6	0.90V					On(5)		
6	1.00V				On(5)			
6	1.25V			On(5)				
6	1.32V		On(5)					
6	1.50V	On(5)						
7	0.75V							On(6)
7	0.80V						On(6)	
7	0.90V					On(6)		
7	1.00V				On(6)			
7	1.25V			On(6)				
7	1.32V		On(6)					
7	1.50V	On(6)						

Table 3: Choosing a reference voltage.

Note: *Make sure that there are never several switches for the same bank turned on simultaneously, i.e. there is only one on(1), on(2) etc. Several closed switches would produce short circuits in the voltage divider resistor network and would therefore produce wrong reference voltages.*

5.2 FPGA Configuration

The FPGAs with Virtex architecture support the following four configuration modes:

- Master Serial Mode
- Slave Serial Mode
- SelectMAP mode
- Boundary-scan mode

The configuration pins (M2, M1, M0) select among these modes with the option in each case of having the IOB pins either pulled up or left floating prior to configuration. The selection codes are listed in *Table 4*.

Mode	J5_5 (M2)	J4_5 (M1)	J3_5 (M0)	CCLK Direction	Bits	Busy/ Dout	Internal Pullups
Master Serial	Yes	Yes	Yes	Out	1	Yes	No
Boundary Scan	-	Yes	-	N/A	1	No	No
SelectMAP	-	-	Yes	In	8	No	No
Slave Serial	-	-	-	In	1	No	No
Master Serial	-	Yes	Yes	Out	1	Yes	Yes
Boundary Scan	Yes	Yes	-	N/A	1	No	Yes

Mode	J5_5 (M2)	J4_5 (M1)	J3_5 (M0)	CCLK Direction	Bits	Busy/ Dout	Internal Pullups
SelectMAP	Yes	-	Yes	In	8	No	Yes
Slave Serial	Yes	-	-	In	1	No	Yes

Table 4: Setting the configuration modes.

An inserted jumper ties the appropriate pin to ground whereas the pin is pulled high if the jumper is removed. Here and in the following tables, a "Yes" in the jumper column means that the jumper is inserted whereas a "–" means that no jumper is plugged in.

5.2.1 Master Serial Mode

In master serial mode, the CCLK output of the FPGA drives a Xilinx Serial PROM that feeds bit-serial data to the DIN input. The FPGA accepts this data on each rising CCLK edge. After the FPGA has been loaded, the data for the next device in a daisy-chain is presented on the DOUT pin after the rising CCLK edge. The preamble is also forwarded to other devices in the daisy chain. SPROM RESET pin is driven by INIT\, and CE\ input is driven by DONE.

The master serial mode is selected by the following jumper settings:

J5_5 (M2)	J4_5 (M1)	J3_5 (M0)	Internal pull-ups on IOB pins
Yes	Yes	Yes	No
-	Yes	Yes	Yes

Table 5: Master serial mode selection.

5.2.1.1 In System Programmable PROMs

The ISP PROM module with SPROMs of the XC18Vxx family is optional. Depending on the size of the FPGA a different sized module is needed. This module is programmable many times over the JTAG. If no module is present, the bypass jumper J28_5 connects the JTAG data input directly with the FPGA. The jumper setting to use this device as the source of configuration data is as follows:

Module Used	J6_5 ("PROM Select")	J28_5 ("No PROM Module")
Yes	Inserted	Removed
No	Removed	Inserted

Table 6: Selecting the XC18V04 ISP PROM module M1_5 as serial configuration data source.

The ISP PROM modules contain a different number of XC18V04 SPROMs, depending on the size of the FPGA. The knowledge of the exact composition is crucial if you want to reprogram the module or if you want to program the FPGA directly in JTAG mode. The module composition and corresponding JTAG chain configuration is given in the following table ('04 is an abbreviation for an XC18V04):

FPGA Type	Module Composition	JTAG Chain
XC2V1000	XC18V04	'04 → FPGA
XC2V1500	2 of XC18V04	'04 → '04 → FPGA
XC2V2000	2 of XC18V04	'04 → '04 → FPGA
XC2V3000	3 of XC18V04	'04 → ... → '04 → FPGA
XC2V4000	4 of XC18V04	'04 → ... → '04 → FPGA
XC2V6000	6 of XC18V04	'04 → ... → '04 → FPGA
XC2V8000	7 of XC18V04	'04 → ... → '04 → FPGA

Table 7: ISP SPROM module composition and JTAG chains.

You can program the module via the JTAG port J2_5. TDI of M1_5 is connected directly with the corresponding pin of J2_5. The TDO output of M1_5 is connected with the TDI input of the FPGA. The pin assignment of the JTAG port is listed in *Table 8*:

Pin of JTAG port J2_5	Signal Name
1	TMS
2	TDI
3	TDO
4	TCK
5	GND
6	3.3V

Table 8: JTAG port pin assignment.

The signal pins TMS, TDI, TDO and TCK are connected over 100 Ω series resistors with the FPGA to protect the inputs from accidentally applied 5V signals.

5.2.2 Slave Serial Mode

In slave serial mode, the FPGA receives configuration data in bit-serial form from a serial PROM or other source of serial configuration data. An external device, e.g. XChecker cable, generates the download clock. Multiple FPGAs can be daisy-chained for configuration from a single source. After a particular FPGA has been configured, the data for the next device is routed to the DOUT pin.

The slave serial mode is selected by the following jumper settings:

J5_5 (M2)	J4_5 (M1)	J3_5 (M0)	Internal pull-ups on IOB pins
-	-	-	No
Yes	-	-	Yes

Table 9: Slave serial mode selection.

Note: *Be sure to disable the SPROM module by removing jumper J6_5 before applying data at the XChecker port.*

5.2.2.1 Configuration via XChecker Port

In slave serial mode, the serial configuration data comes from the XChecker port J1_5. Either a parallel or a serial cable may be used. Due to the 3.3V cable supply voltage, we recommend to use an appropriate cable (Xilinx order number: HW-XCH3V). Nevertheless, experiments with 5V cables showed, that these cables work well down to 3V, parallel cables even down to 2V. The circumstances under which a certain cable will work depend on many factors, including the PC used. Whether a cable that is specified for 5V operation will work is not guaranteed.

In any case we strongly recommend using the MultiLinx cable that has the additional advantage of being able to use the USB bus. This results in a large increase of download speed.

In addition to the slave serial mode setting J6_5 must be removed:

J6_5 ("PROM Select")
Removed

Table 10: Jumper setting for XChecker configuration.

The pin assignments of the XChecker port connector are listed in the following table:

Pin of XChecker port J1_5	Signal Name
1	PROG\
2	DONE
3	INIT\
4	CCLK
5	DATA
6	3.3V
7	GND

Table 11: XChecker port pin assignment.

The signal pins PROG\, DONE, INIT\, CCLK and DATA are connected over 100 Ω series resistors with the FPGA to protect the inputs from accidentally applied 5V signals.

5.2.3 SelectMAP Mode

The SelectMAP mode is the fastest configuration option. Byte-serial data is written into the FPGA with a BUSY flag controlling the flow of data. An external data source provides a byte stream, CCLK, a Chip Select (CS) signal and a Write signal (WRITE). If BUSY is asserted (High) by the FPGA, the data must be held until BUSY goes Low. Data can also be read using the SelectMAP mode. If WRITE is not asserted, configuration data is read out of the FPGA as part of a readback operation.

The SelectMAP mode is selected by the following jumper settings:

J5_5 (M2)	J4_5 (M1)	J3_5 (M0)	Internal pull-ups on IOB pins
-	-	Yes	No
Yes	-	Yes	Yes

Table 12: SelectMAP mode selection.

The byte-serial data is fed from an external source to the SelectMAP port J7_5 using the following pin assignments:

Pin of SelectMAP port J7_5	Signal Name
1	D0
2	D1
3	D2
4	D3
5	D4
6	D5
7	D6
8	D7
9	BUSY/DOUT
10	WRITE\
11	CS\
12	GND

Table 13: SelectMAP port pin assignment.

The signal pins D0 to D7, BUSY/DOUT, WRITE\ and CS\ are connected over 100 Ω series resistors with the FPGA to protect the inputs from accidentally applied 5V signals.

5.2.4 Boundary Scan Mode

In the boundary-scan mode, no non-dedicated pins are required, configuration being done entirely through the IEEE 1149.1 Test Access Port. Configuration and readback is always available. The boundary-scan mode simply locks out the other modes.
The boundary scan mode is selected by the following jumper settings:

J5_5 (M2)	J4_5 (M1)	J3_5 (M0)	Internal pull-ups on IOB pins
-	Yes	-	No
Yes	Yes	-	Yes

Table 14: Boundary scan mode selection.

The pin assignment of the JTAG port J2_5 is listed in *Table 8*.

5.3 Clock

Eight primary clock pins (GCLK0P to GCLK7P) and eight secondary clock pins (GCLK0S to GCLK7S) are routed to coaxial SMB connectors. *GCLK0P* and *GCLK1P* may get the clock signal either from an internal crystal oscillator or from an external source, see *Table 15*.

J3_7 (GCLK0P)	J4_7 (GCLK1P)	GCLK0P Source	GCLK1P Source
2-3	2-3	internal U1_7	internal U2_7
2-3	1-2	internal U1_7	external J2_7
1-2	2-3	external J1_7	internal U2_7
1-2	1-2	external J1_7	external J2_7

Table 15: Choice of the clock sources for GCLK0P and GCLK1P.

5.3.1 External Clock

All external clock signals are feed through coaxial connectors. These connectors are arranged at the four corners of the board. This kind of clock supply, together with an impedance controlled FPGA clock input and the matching trace impedance of the PCB, guarantees clean clock signals. Since the clock inputs of the FPGA can also be configured as general I/Os you are able use this connectors as clock outputs too. The assignment of the clock signals to the coaxial connectors is listed in Table 16.

Signal Clock Name	Direct Clock Connector	Signal Name	FF1152 Pin XC2V3000-8000	FF896 Pin XC2V1000-2000
GCLK0P	J1_7	IO_L96P_4/GCLK0P	AK17	AH15
GCLK1P	J2_7	IO_L95N_1/GCLK1P	H17	F15
GCLK2P	J7_7	IO_L95P_4/GCLK2P	AG17	AE15
GCLK3P	J8_7	IO_L96N_1/GCLK3P	E17	C15
GCLK4P	J9_7	IO_L95P_5/GCLK4P	AF18	AD16
GCLK5P	J13_7	IO_L96N_0/GCLK5P	E19	C17
GCLK6P	J14_7	IO_L96P_5/GCLK6P	AK19	AH17
GCLK7P	J15_7	IO_L95N_0/GCLK7P	K18	H16
GCLK0S	J5_7	IO_L95P_1/GCLK0S	H16	F14
GCLK1S	J6_7	IO_L96N_4/GCLK1S	AK16	AH14
GCLK2S	J10_7	IO_L96P_1/GCLK2S	E16	C14
GCLK3S	J11_7	IO_L95N_4/GCLK3S	AF17	AD15
GCLK4S	J12_7	IO_L96P_0/GCLK4S	E18	C16
GCLK5S	J16_7	IO_L95N_5/GCLK5S	AG18	AE16
GCLK6S	J17_7	IO_L95P_0/GCLK6S	J18	G16
GCLK7S	J18_7	IO_L96N_5/GCLK7S	AK18	AH16

Table 16: External clock signal connectors and FPGA pin assignment.

5.3.2 Internal Clock (Crystal Oscillators)

Since the clock frequency depends strongly on the application, the oscillators must be exchangeable. The oscillators socket can hold DIL-8 or DIL-14 packages. Pin 1 is common for both types of packages.

5.3.2.1 VCXO with Feedback Loop

Oscillators of the VCXO type need a control signal at pin 1 (U_c). To get a closed feedback loop, this signal must be connected (via FPGA) to U_{out}. You have the possibility to build an RC loop filter be mounting R1_7, C2_7 and R2_7, C3_7. This can be useful if you want to generate the oscillator control voltage with a pulse code modulated digital signal.

Crystal Oscillator	$U_{control}$ Signal	Clock source for
U1_7	OSC1_CNTL	GCLK0P
U2_7	OSC2_CNTL	GCLK1P

Table 17: Crystal oscillator control signals and usage.

5.4 Digitally Controlled Impedance (DCI)

The Virtex-II FPGA provides controlled impedance drivers and on-chip termination for single-ended I/Os. This eliminates the need for external resistors and improves signal integrity. The board is designed such that the signal lines have a characteristic impedance of about 50 Ω. Two external reference resistors of 51 Ω are connected to the two dual-function pins (VRN and VRP) on each bank to set the DCI accordingly.

5.5 Reset and Voltage Supervision

U4_4 works as a reset and voltage supervision circuit. A functional reset can be issued at any time by pressing the push button S1_4. The button is connected to the voltage supervisor circuit U4_4, which in turn generates a reset pulse. A reset pulse is also generated whenever VCCINT drops below a predefined threshold of 1.3V and on power up. The pulse duration is approximately 2ms, the polarity may be selected with jumper J21_5 to be either active low (“L” position) or active high (“H” position).

Signal Name	FF1152 Pin XC2V3000-8000	FF896 Pin XC2V1000-2000
XRESET	AH22	AF20

Table 18: Manual and voltage supervisor reset signal connection with FPGA bank 5.

Note: *A manual reset initializes the internal circuits of the FPGA (registers, counters, finite state machines etc.) and must be implemented in the design appropriately. There is no dedicated reset pin on the FPGA.*

5.6 Real Time Clock (RTC)

The RTC device U3_4 (RTC-8564JE from Epson) contains an I^2C interface that is connected with the FPGA. This interface consists of a clock line (SCL_RTC) and a data line (SDA_RTC). The RTC slave address on this bus is 1010001. There is also an interrupt output (IRQ_RTC) and a square wave output (SQW_RTC) that are connected with the FPGA. A lithium battery sustains the operation of the RTC when no external power is applied. This battery also keeps the DES key RAM of the FPGA from loosing its data.

The following table summarizes the connections with the FPGA:

Signal Name	RTC Pin U3_4	FF1152 Pin XC2V3000-8000	FF896 Pin XC2V1000-2000
SCL_RTC	6	AM16	AK14
SDA_RTC	7	AJ12	AG10
IRQ_RTC	10	AL16	AJ14
SQW_RTC	5	AJ15(3)	AG13

Table 19: RTC to FPGA connections. Pins marked with (3) are not available on the XC2V3000.

Please consult the data sheet of the RTC-8564 chip for information about internal registers and their programming via the I^2C interface.

5.7 Serial Interface (RS-232, RS-422)

The 9 pole female D-Sub connector J1_11 and the transceiver device U1_11 provide a mean to connect serial devices like a PC to the prototyping board. U1_11 performs the voltage level translation and ESD protection of the RxD and TxD lines. These signals are named RXD0 and TXD0 on the FPGA side of the transceiver. The UART functionality must be implemented in the FPGA (there exist IP cores, see also XAPP 223).

The following tables summarize the involved signals:

Signal Name	U1_11 Pin	FF1152 Pin XC2V3000-8000	FF896 Pin XC2V1000-2000
RXD0	9	AJ26	AG24
TXD0	11	AM28	AK26

Table 20: RS-232 Transceiver to FPGA connections.

Signal Name	Female D-Sub 9 Connector Pin	Transceiver Pin U1_11
RXD (input)	3	8 (R1IN)
TXD (output)	2	13 (T1OUT)
GND	5	1, 12, 14

Table 21: RS-232 Connector to Transceiver connections.

Alternatively to the single ended ground referenced signals (RS-232) you can use the differential signal standard RS-422. The advantage of this arrangement is the much improved bit rate that can exceed 10Mb/s. The differential driver U7_11 is implemented by a DS26LV31 line driver and the differential line receiver U8_11 by a DS26LV32. The inputs of the receiver are terminated with a 100 Ω resistor.

FPGA pin assignments for the differential driver/receiver are as follows:

Signal Name	Receiver/ Driver Pin	FF1152 Pin XC2V3000-8000	FF896 Pin XC2V1000-2000
RXD1	U8_11(5)	AJ16	AG14
TXD1	U7_11(7)	AJ27	AG25

Table 22: RS-422 Driver/Receiver to FPGA connections.

The female D-Sub 9 connector J1_11 is configured for RS-232 by default, but can be reconfigured for RS-422 by

- removing the 0 Ω resistors R13_11, R14_11, R15_11 and R29_11,
- and inserting 0 Ω resistors R16_11 to R26_11.

The RS-422 signals are always available on the 0.1" header connector J9_11, independent on the configuration of J1_11.
The RS-422 signals on the D-Sub 9 connector (after reconfiguration) and the 0.1" header connector are as follows:

RS-422 Signal Name	J9_11 Header Connector Pin	J1_11 D-Sub 9 Connector Pin
CTS-	2	3
CTS+	1	2
RXD-	4	5
RXD+	3	4
RTS-	6	7
RTS+	5	6
TXD-	8	9
TXD+	7	8
GND	9	1
3.3V	10	

Table 23: RS-422 Signals on the female D-Sub 9 and the 0.1" header connector.

The differential drivers/receivers are connected to the FPGA with a non-differential signal:

RS-422 Signal Pair	Net Name	FF1152 Pin XC2V3000-8000	FF896 Pin XC2V1000-2000
RXD+, RXD-	RXD1	AJ16	AG14
TXD+, TXD-	TXD1	AJ27	AG25
CTS+, CTS-	RXD0	AJ26	AG24
RTS+, RTS-	TXD0	AM28	AK26

Table 24: RS-422 Driver/Receiver connection with FPGA.

5.8 Temperature Sensor

The temperature sensor (ADM1021 from Analog Devices) is a digital thermometer that reports the temperature of both a remote sensor and its own package. The remote sensor is a diode-connected transistor and connects directly to the temperature sensing diode in the FPGA package.

The 2-wire serial interface accepts standard System Management Bus (SMBus®) Write Byte, Read Byte, Send Byte, and Receive Byte commands to program the alarm thresholds and to read temperature data. The slave address is 0011000. The data format is 7 bits plus sign, with each bit corresponding to 1°C, in two's complement format. Measurements can be done automatically and autonomously, with the conversion rate programmed by the user or programmed to operate in a single-shot mode.

The connection with the FPGA is given in the following table:

Signal Name	Sensor U1_1 Pin	FF1152 Pin XC2V3000-8000	FF896 Pin XC2V1000-2000
SMBCLK	14	AL6	AJ4
SMBDATA	12	AH10	AF8
XALERT	11	AM17	AK15

Table 25: Temperature sensor to FPGA connections.

Please consult the MAX1617 data sheet for more information about using and programming this chip.

5.9 User Buttons

Twelve user buttons S3_6 to S6_6, S9_6 to S12_6 and S17_6 to S19_6 are available for arbitrary purposes. A pressed button ties the connected FPGA pin to ground while the pin is pulled to 3.3V if the button is released.

Button	Label or Color	FF1152 Pin XC2V3000-8000	FF896 Pin XC2V1000-2000
S3_6	Yellow	AF22	AD20
S4_6	Blue	AK27	AH25
S5_6	0	AG23	AE21
S6_6	1	AF24	AD22
S9_6	2	AL19	AJ17
S10_6	3	AM20	AK18
S11_6	4	AM19	AK17
S12_6	5	AJ18	AG16
S17_6	6	AJ19	AG17
S18_6	7	AM29	AK27
S19_6	8	AH24	AF22
S20_6	9	AK26	AH24

Table 26: User button connection with FPGA bank 5.

The connection of a user button with the FPGA is routed over a 510 Ω resistor. A pressed button does therefore not harm the FPGA if the corresponding pin is accidentally configured as output.

5.10 Eight Position DIP Switches

The two eight-position DIP switches S13_6 and S21_6 can be used for application specific purposes. In the *On* position the connected FPGA pin is tied to ground. In the *Off* position the connected FPGA pin is pulled to 3.3V via a resistor.

The switches are connected to the FPGA via resistors of 510 Ω. Owing to these resistors, a switch closed to ground does not harm the FPGA if the corresponding pin is accidentally configured as output.

The assignment of the switches to the FPGA pins on bank 5 is as follows:

Switch S13_6	Signal Name	FF1152 Pin XC2V3000-8000	FF896 Pin XC2V1000-2000
1	DIPSW0	AN28	
2	DIPSW1	AN31	
3	DIPSW2	AP28	
4	DIPSW3	AN29	
5	DIPSW4	AN27	
6	DIPSW5	AP26	
7	DIPSW6	AN26[3]	
8	DIPSW7	AN25[3]	

Table 27: Signals on the eight position DIP switch S13_6. Pins marked with [3] are not available on the XC2V3000. This DIP switch is not available on XC2V2000 and smaller devices.

Switch S21_6	Signal Name	FF1152 Pin XC2V3000-8000	FF896 Pin XC2V1000-2000
1	DIPSW8	AF23	AD21
2	DIPSW9	AM27	AK25
3	DIPSW10	AM26	AK24
4	DIPSW11	AL27	AJ25
5	DIPSW12	AL26	AJ24
6	DIPSW13	AH26	AF24
7	DIPSW14	AJ25	AG23
8	DIPSW15	AH25	AF23

Table 28: Signals on the eight position DIP switch S21_6.

5.11 Light Emitting Diodes (LEDs)

The sixteen LEDs D1_6 to D16_6 are intended as optical indicators for the display of status information. They turn on whenever the corresponding FPGA output is low.

D1_5 is connected to the DONE pin of the FPGA.

Power indicator LEDs are D2_4 (VCCAUX), D5_4 (VCCO), D6_4 (VCCINT) and D4_4 (input power). The DONE LED turns on at the end of a successful bit stream download.
The general purpose LEDs D1_6 to D16_6 are connected to the FPGA according to the following table:

LED	Signal Name	FF1152 Pin XC2V3000-8000	FF896 Pin XC2V1000-2000
D1_6	LED0	AJ23	AG21
D2_6	LED1	AG21	AE19
D3_6	LED2	AG22	AE20
D4_6	LED3	AK24	AH22
D5_6	LED4	AK25	AH23
D6_6	LED5	AL25	AJ23
D7_6	LED6	AL24	AJ22
D8_6	LED7	AH23	AF21
D9_6	LED8	AE21	AC19(1)
D10_6	LED9	AE20	AC18(1)
D11_6	LED10	AP31	
D12_6	LED11	AP30	
D13_6	LED12	AN24	
D14_6	LED13	AN23	
D15_6	LED14	AM33	
D16_6	LED15	AN30	

Table 29: General purpose LED connection with FPGA bank 5. Pins marked with (1) are not available on the XC2V1000.

5.12 Liquid Crystal Display (LCD)

A 4 line, 20 character liquid crystal display with parallel interface provides an advanced mean for displaying debugging information during development. The integrated display controller KS0073 (Samsung) contains a simple parallel interface with 8 data bits and 4 control lines. It can be initialized with a few 8-bit instruction writes. Characters can then be displayed by simply writing the equivalent 8-bit code to the display controller RAM.

The LCD module is connected to general I/Os of bank 3 that are also accessible on the connector J1_9. The following table shows the FPGA pin assignments:

LCD Signal	Signal Name	FF1152 Pin XC2V3000-8000	FF896 Pin XC2V1000-2000
RS	IO_L43P_3	AG3	AE1
R_XW	IO_L24P_3	AG6	AE4
E	IO_L22P_3	AG7	AE5
XRES	IO_L25P_3	AH5	AF3
D0	IO_L43N_3	AF3	AD1
D1	IO_L24N_3	AF6	AD4
D2	IO_L22N_3	AF7	AD5
D3	IO_L03P_3	AF11	AD9
D4	IO_L23N_3	AH3	AF1
D5	IO_L25N_3	AG4	AE2
D6	IO_L01N_3	AF10	AD8
D7	IO_L23P_3	AJ3	AG1

Table 30: LCD module connections with FPGA.

Note: *In order to use the LCD module, bank 3 must be configured with an IO standard that uses an output driver voltage of 3.3V and that is compatible with LVTTL or LVCMOS signal levels.*

The green-yellow back light is powered by a constant current source that connects directly to the input power voltage. The contrast of the display can be adjusted with the potentiometer R12_11.

5.13 Text-to-Speech Processor (TTSP)

The text-to-speech processor U5_11 (WTS701 from Winbond) and the audio power amplifier U4_11 (LM4861 or LM4901 from National Semiconductors) form a text-to-speech subunit. It accepts ASCII input via a SPI port and converts it to spoken audio. The text-to-speech conversion is achieved by the WTS701 by processing the incoming text into a phonetic representation that is then mapped to a corpus of naturally spoken word parts. The synthesis algorithm of this chip attempts to use the largest possible word unit in the appropriate context to maximize natural sounding speech quality. The speech units are stored uncompressed in a non-volatile analog storage array within the WTS701. The audio output is amplified by the audio amplifier to deliver sufficient power to an 8 Ω speaker. An external speaker can be connected to J4_11.

Note: *If you connect an external speaker, be sure to disconnect the onboard speaker to avoid damage to the audio amplifier due to a too low load resistance.*

The text-to-speech unit can be driven either internally by some FPGA I/Os on bank 0 and 1 or externally by feeding driving signals to J5_11. Jumper settings and signal assignments for both of these possibilities are described in the next two subsections.

Note: *In order to drive the text-to-speech unit by the FPGA, banks 0 and 1 must be configured with an IO standard that uses an output driver voltage of 3.3V and that is compatible with LVTTL or LVCMOS signal levels.*

5.13.1 Internal Driver (FPGA)

If you want to use the FPGA to drive the text-to-speech processor, you must insert the jumpers J2_11, J6_11 and all eight jumpers of J7_11. J3_11 may also be inserted if you want to use the shutdown function of the power amplifier. The FPGA pin assignments are now as follows:

TTSP Signal	Signal Name	FF1152 Pin XC2V3000-8000	FF896 Pin XC2V1000-2000
XTAL1	IO_L95N_0 /GCLK7P	K18	H16
SS	IO_L05N_1	H11	F9
SCLK	IO_L06N_1	D6	B4
MOSI	IO_L06P_1	C6	A4
MISO	IO_L04N_1	D8	B6
CS	IO_L23P_1	G11	E9
INT	IO_L27P_1	E10	C8
R_B	IO_L93P_0	F19	D17
RESET	IO_L93N_0	F18	D16
AMP_SD	IO_L91P_0	D18	B16

Table 31: Text-to-Speech unit connections with FPGA.

5.13.2 External Driver Hardware

If you want to drive the TTSP by external hardware, you must remove the jumpers J2_11, J3_11, J16_11, and all eight jumpers of J7_11. You can now connect the external signals to J5_11:

TTSP Signal	J5_11 Connector Pin
R_B	1
RESET	2
SP1	3
SP2	4
ATTCAP	5
AUXOUT	6
SCLK	7
SS	8
MOSI	9
MISO	10
INT	11
XTAL1	12
XTAL2	13
VDX	14
VFS	15
VCLK	16
GND	18, 20
3.3V	17, 19

Table 32: Driving the Text-to-Speech unit by external hardware through the J5_11 connector.

5.14 High Speed Asynchronous SRAM

Two 256KBx16 high speed (12ns cycle time) asynchronous static RAM chips (U2_11, U3_11) belong to the standard equipment of this development board for a XC2V4000 or larger FPGA. For smaller FPGAs (XC2V1000 to XC2V3000) the RAMs can not be used because of missing I/O pins on the FPGA. Address, data and control signals are separately accessible from the FPGA such that both chips may be operated independently of each other. This way you can implement a double speed RAM by accessing the two RAM chips in an interleaved manner. You can also realize a single 512KBx16 or 256KBx32 RAM.

The connections with the FPGA are listed in the following tables:

Signal Name	RAM (U2_11) Pin Name (Number)	FF1152 Pin XC2V3000-8000	FF896 Pin XC2V1000-2000
A0L_Bank4	A0 (1)	AN4	
A1L_Bank4	A1 (2)	AE12	AC10
A2L_Bank4	A2 (3)	AE13	AC11
A3L_Bank4	A3 (4)	AM9	AK7
A4L_Bank4	A4 (5)	AL8	AJ6
A5L_Bank4	A5 (18)	AP5	
A6L_Bank4	A6 (19)	AP4	
A7L_Bank4	A7 (20)	AG11	AE9
A8L_Bank4	A8 (21)	AG12	AE10
A9L_Bank4	A9 (22)	AN7	
A10L_Bank4	A10 (23)	AL10	AJ8
A11L_Bank4	A11 (24)	AL9	AJ7
A12L_Bank4	A12 (25)	AF12	AD10
A13L_Bank4	A13 (26)	AF13	AD11
A14L_Bank4	A14 (27)	AK10	AH8
A15L_Bank4	A15 (42)	AK11	AH9
A16L_Bank4	A16 (43)	AP7	
XADSL_Bank4	A17 (44)	AN8	
IO0L_Bank4	I/O1 (7)	AM6	AK4
IO1L_Bank4	I/O2 (8)	AM8	AK6
IO2L_Bank4	I/O3 (9)	AM7	AK5
IO3L_Bank4	I/O4 (10)	AN3	
IO4L_Bank4	I/O5 (13)	AM2	
IO5L_Bank4	I/O6 (14)	AJ10	AG8
IO6L_Bank4	I/O7 (15)	AJ9	AG7
IO7L_Bank4	I/O8 (16)	AH9	AF7
IO0R_Bank4	I/O9 (29)	AN9(3)	
IO1R_Bank4	I/O10 (30)	AN12	
IO2R_Bank4	I/O11 (31)	AN11	
IO3R_Bank4	I/O12 (32)	AE14	AC12(1)
IO4R_Bank4	I/O13 (35)	AE15	AC13(1)
IO5R_Bank4	I/O14 (36)	AJ13	AG11(1)
IO6R_Bank4	I/O15 (37)	AL13	AJ11(1)
IO7R_Bank4	I/O16 (38)	AL12	AJ10(1)
XCE0L_Bank4	XCS (6)	AH13	AF11
XOEL_Bank4	XOE (41)	AJ11	AG9
XCNTRSTL_Bank4	XLB (39)	AG14	AE12
XCNTENL_Bank4	XUB (40)	AM11	AK9
R/XWRL_Bank4	XWE (17)	AP9	

Table 33: Connections of the SRAM chip U2_11 with the FPGA. Pins marked with (1), (5), (3) are not available on the XC2V1000, XC2V1500 or XC2V3000, respectively.

Signal Name	RAM (U3_11) Pin Name (Number)	FF1152 Pin XC2V3000-8000	FF896 Pin XC2V1000-2000
A0R_Bank4	A0 (1)	AF15	AD13(1)
A1R_Bank4	A1 (2)	AM13	AK11(1)
A2R_Bank4	A2 (3)	AM12	AK10(1)
A3R_Bank4	A3 (4)	AP12	
A4R_Bank4	A4 (5)	AP11	
A5R_Bank4	A5 (18)	AG15	AE13(1) (5)
A6R_Bank4	A6 (19)	AG16	AE14(1) (5)
A7R_Bank4	A7 (20)	AN14	
A8R_Bank4	A8 (21)	AP14	
A9R_Bank4	A9 (22)	AP13	
A10R_Bank4	A10 (23)	AD16	AB14(1) (5)
A11R_Bank4	A11 (24)	AD17	AB15(1) (5)
A12R_Bank4	A12 (25)	AK14	AH12(1)
A13R_Bank4	A13 (26)	AK13	AH11(1)
A14R_Bank4	A14 (27)	AN16(3)	
A15R_Bank4	A15 (42)	AP15(3)	
A16R_Bank4	A16 (43)	AE16(3)	AC14
XADSR_Bank4	A17 (44)	AH16(3)	AF14(1) (5)
IO0L_Bank5	I/O1 (7)	AL18	AJ16
IO1L_Bank5	I/O2 (8)	AJ21	AG19
IO2L_Bank5	I/O3 (9)	AJ20	AG18
IO3L_Bank5	I/O4 (10)	AH19	AF17(1) (5)
IO4L_Bank5	I/O5 (13)	AH18	AF16(1) (5)
IO5L_Bank5	I/O6 (14)	AP20	
IO6L_Bank5	I/O7 (15)	AL21(3)	AJ19(1) (5)
IO7L_Bank5	I/O8 (16)	AL20(3)	AJ18(1) (5)
IO0R_Bank5	I/O9 (29)	AD18	AB16(1) (5)
IO1R_Bank5	I/O10 (30)	AD19	AB17(1) (5)
IO2R_Bank5	I/O11 (31)	AN22	
IO3R_Bank5	I/O12 (32)	AN21	
IO4R_Bank5	I/O13 (35)	AH20	AF18(1) (5)
IO5R_Bank5	I/O14 (36)	AG19	AE17(1) (5)
IO6R_Bank5	I/O15 (37)	AG20	AE18(1) (5)
IO7R_Bank5	I/O16 (38)	AP24	
XCE0R_Bank4	XCS (6)	AH15(3)	AF13(1) (5)
XOER_Bank4	XOE (41)	AN17(3)	
XCNTRSTR_Bank4	XLB (39)	AL14(3)	AJ12(1) (5)
XCNTENR_Bank4	XUB (40)	AL17	AJ15
R/XWRR_Bank4	XWE (17)	AH17(3)	AF15(1) (5)

Table 34: Connections of the SRAM chip U3_11 with the FPGA. Pins marked with (1), (5), (3) are not available on the XC2V1000, XC2V1500 or XC2V3000, respectively.

5.15 Dual Port RAM Option

This option is only possible with XC2V4000 and larger devices. They are not included in the standard version of this board. The dual port RAMs (DPRs) U1_10 and U2_10 are optional. They share address, data and control signals with the high speed asynchronous SRAMs. Only the chip enable signals are separate for all RAM chips. You can only use two RAM chips at the same time, either both DPRs, both SRAMS, the first DPR and the second SRAM or the second DPR and the first SRAM. In addition, both DPRs share common address lines.

The connections with the FPGA are listed in the following tables:

Signal Name	RAM (U1_10) Pin Name (Number)	FF1152 Pin XC2V3000-8000	FF896 Pin XC2V1000-2000
A0L_Bank4	A0L (92)	AN4	
A1L_Bank4	A1L (93)	AE12	AC10
A2L_Bank4	A2L (94)	AE13	AC11
A3L_Bank4	A3L (95)	AM9	AK7
A4L_Bank4	A4L (96)	AL8	AJ6
A5L_Bank4	A5L (97)	AP5	
A6L_Bank4	A6L (98)	AP4	
A7L_Bank4	A7L (3)	AG11	AE9
A8L_Bank4	A8L (4)	AG12	AE10
A9L_Bank4	A9L (5)	AN7	
A10L_Bank4	A10L (6)	AL10	AJ8
A11L_Bank4	A11L (7)	AL9	AJ7
A12L_Bank4	A12L (8)	AF12	AD10
A13L_Bank4	A13L (9)	AF13	AD11
A14L_Bank4	A14L (10)	AK10	AH8
A15L_Bank4	A15L (11)	AK11	AH9
A16L_Bank4	A16L (12)	AP7	
A0R_Bank4	A0R (83)	AF15	AD13(1)
A1R_Bank4	A1R (82)	AM13	AK11(1)
A2R_Bank4	A2R (81)	AM12	AK10(1)
A3R_Bank4	A3R (80)	AP12	
A4R_Bank4	A4R (79)	AP11	
A5R_Bank4	A5R (78)	AG15	AE13(1) (5)
A6R_Bank4	A6R (77)	AG16	AE14(1) (5)
A7R_Bank4	A7R (73)	AN14	
A8R_Bank4	A8R (72)	AP14	
A9R_Bank4	A9R (71)	AP13	
A10R_Bank4	A10R (70)	AD16	AB14(1) (5)
A11R_Bank4	A11R (69)	AD17	AB15(1) (5)
A12R_Bank4	A12R (68)	AK14	AH12(1)
A13R_Bank4	A13R (67)	AK13	AH11(1)
A14R_Bank4	A14R (66)	AN16(3)	
A15R_Bank4	A15R (65)	AP15(3)	
A16R_Bank4	A16R (64)	AE16(3)	AC14
IO0L_Bank4	I/O0L (36)	AM6	AK4
IO1L_Bank4	I/O1L (35)	AM8	AK6
IO2L_Bank4	I/O2L (33)	AM7	AK5
IO3L_Bank4	I/O3L (32)	AN3	
IO4L_Bank4	I/O4L (31)	AM2	
IO5L_Bank4	I/O5L (30)	AJ10	AG8
IO6L_Bank4	I/O6L (29)	AJ9	AG7
IO7L_Bank4	I/O7L (28)	AH9	AF7
IO0R_Bank4	I/O0R (39)	AN9(3)	
IO1R_Bank4	I/O1R (40)	AN12	
IO2R_Bank4	I/O2R (41)	AN11	
IO3R_Bank4	I/O3R (43)	AE14	AC12(1)
IO4R_Bank4	I/O4R (44)	AE15	AC13(1)
IO5R_Bank4	I/O5R (45)	AJ13	AG11(1)
IO6R_Bank4	I/O6R (46)	AL13	AJ11(1)
IO7R_Bank4	I/O7R (47)	AL12	AJ10(1)
XCE0L_Bank4	XCE0L (18)	AH13	AF11
CE1L_Bank4	CE1L (19)	AH12	AF10
XOEL_Bank4	XOEL (22)	AJ11	AG9
R/XWRL_Bank4	R/XWL (21)	AP9	
XADSL_Bank4	XADSL (89)	AN8	
XFT/PIPEL_Bank4	XFT/PIPEL (23)	AG13	AE11
XCNTRSTL_Bank4	XCNTRSTL (20)	AG14	AE12
XCNTENL_Bank4	XCNTENL (91)	AM11	AK9
CLKL_Bank4	CLKL (90)	AL11	AJ9
XCE0R_Bank4	XCE0R (58)	AH15(3)	AF13(1) (5)
CE1R_Bank4	CE1R (57)	AP17(3)	
XOER_Bank4	XOER (54)	AN17(3)	
R/XWRR_Bank4	R/XWR (55)	AH17(3)	AF15(1) (5)
XADSR_Bank4	XADSR (86)	AH16(3)	AF14(1) (5)
XFT/PIPER_Bank4	XFT/PIPER (53)	AL15(3)	AJ13(1) (5)
XCNTRSTR_Bank4	XCNTRSTR (56)	AL14(3)	AJ12(1) (5)
XCNTENR_Bank4	XCNTENR (84)	AL17	AJ15
CLKR_Bank4	CLKR (85)	AJ17	AG15

Table 35: Connections of the DPR chip U1_10 with the FPGA. Pins marked with (1), (5), (3) are not available on the XC2V1000, XC2V1500 or XC2V3000, respectively.

Signal Name	RAM (U2_10) Pin Name (Number)	FF1152 Pin XC2V3000-8000	FF896 Pin XC2V1000-2000
A0L_Bank4	A0L (92)	AN4	
A1L_Bank4	A1L (93)	AE12	AC10
A2L_Bank4	A2L (94)	AE13	AC11
A3L_Bank4	A3L (95)	AM9	AK7
A4L_Bank4	A4L (96)	AL8	AJ6
A5L_Bank4	A5L (97)	AP5	
A6L_Bank4	A6L (98)	AP4	
A7L_Bank4	A7L (3)	AG11	AE9
A8L_Bank4	A8L (4)	AG12	AE10
A9L_Bank4	A9L (5)	AN7	
A10L_Bank4	A10L (6)	AL10	AJ8
A11L_Bank4	A11L (7)	AL9	AJ7
A12L_Bank4	A12L (8)	AF12	AD10
A13L_Bank4	A13L (9)	AF13	AD11
A14L_Bank4	A14L (10)	AK10	AH8
A15L_Bank4	A15L (11)	AK11	AH9
A16L_Bank4	A16L (12)	AP7	
A0R_Bank4	A0R (83)	AF15	AD13
A1R_Bank4	A1R (82)	AM13	AK11(1)
A2R_Bank4	A2R (81)	AM12	AK10(1)
A3R_Bank4	A3R (80)	AP12	
A4R_Bank4	A4R (79)	AP11	
A5R_Bank4	A5R (78)	AG15	AE13(1) (5)
A6R_Bank4	A6R (77)	AG16	AE14(1) (5)
A7R_Bank4	A7R (73)	AN14	
A8R_Bank4	A8R (72)	AP14	
A9R_Bank4	A9R (71)	AP13	
A10R_Bank4	A10R (70)	AD16	AB14(1) (5)
A11R_Bank4	A11R (69)	AD17	AB15(1) (5)
A12R_Bank4	A12R (68)	AK14	AH12(1)
A13R_Bank4	A13R (67)	AK13	AH11(1)
A14R_Bank4	A14R (66)	AN16(3)	
A15R_Bank4	A15R (65)	AP15(3)	
A16R_Bank4	A16R (64)	AE16(3)	AC14
IO0L_Bank5	I/O0L (36)	AL18	AJ16
IO1L_Bank5	I/O1L (35)	AJ21	AG19
IO2L_Bank5	I/O2L (33)	AJ20	AG18
IO3L_Bank5	I/O3L (32)	AH19	AF17(1) (5)
IO4L_Bank5	I/O4L (31)	AH18	AF16(1) (5)
IO5L_Bank5	I/O5L (30)	AP20	
IO6L_Bank5	I/O6L (29)	AL21(3)	AJ19(1) (5)
IO7L_Bank5	I/O7L (28)	AL20(3)	AJ18(1) (5)
IO0R_Bank5	I/O0R (39)	AD18	AB16(1) (5)
IO1R_Bank5	I/O1R (40)	AD19	AB17(1) (5)
IO2R_Bank5	I/O2R (41)	AN22	
IO3R_Bank5	I/O3R (43)	AN21	
IO4R_Bank5	I/O4R (44)	AH20	AF18(1) (5)
IO5R_Bank5	I/O5R (45)	AG19	AE17(1) (5)
IO6R_Bank5	I/O6R (46)	AG20	AE18(1) (5)
IO7R_Bank5	I/O7R (47)	AP24	
XCE0L_Bank5	XCE0L (18)	AM21(3)	AK19(1) (5)
CE1L_Bank5	CE1L (19)	AN18(3)	
XOEL_Bank5	XOEL (22)	AP18(3)	
R/XWRL_Bank5	R/XWL (21)	AN19(3)	
XADSL_Bank5	XADSL (89)	AE18(3)	AC16
XFT/PIPEL_Bank5	XFT/PIPEL (23)	AE19(3)	AC17
XCNTRSTL_Bank5	XCNTRSTL (20)	AP22(3)	
XCNTENL_Bank5	XCNTENL	AP21(3)	
	(91)		
CLKL_Bank5	CLKL (90)	AK22	AH20(1)
XCE0R_Bank5	XCE0R (58)	AP23	
CE1R_Bank5	CE1R (57)	AL23	AJ21(1)
XOER_Bank5	XOER (54)	AL22	AJ20(1)
R/XWRR_Bank5	R/XWR (55)	AF20	AD18(1)
XADSR_Bank5	XADSR (86)	AF21	AD19(1)
XFT/PIPER_Bank5	XFT/PIPER (53)	AM24	AK22(1)
XCNTRSTR_Bank5	XCNTRSTR (56)	AM23	AK21(1)
XCNTENR_Bank5	XCNTENR (84)	AJ22	AG20(1)
CLKR_Bank5	CLKR (85)	AJ24	AG22

Table 36: Connections of the DPR chip U2_10 with the FPGA. Pins marked with (1), (5), (3) are not available on the XC2V1000, XC2V1500 or XC2V3000, respectively.

5.16 Signals on ERmet® Connectors

All general I/O signals of bank 0,1,2,3,6,7 are routed to header connectors. This does not include the VREF pins that are fixed to the bank reference voltage.

The tables in *Appendix A: Signals on ERmet® Connectors* show the connections of the general I/O FPGA pins to the ERmet® 2mm Hard Metric connectors.

5.16.1 LVDS Signal Assignment to Connector J2_8

This connector is the differential signal connector. A total of 60 LVDS pairs from bank 0 and bank 1 are accessible here.

5.16.2 Bank 2 Signal Assignment to Connector J3_8

This connector contains all ground referenced signals (general I/Os) of bank 2.

5.16.3 Bank 3 Signal Assignment to Connector J1_9

This connector contains all ground referenced signals (general I/Os) of bank 3.

5.16.4 Bank 6 Signal Assignment to Connector J2_9

This connector contains all ground referenced signals (general I/Os) of bank 6.

5.16.5 Bank 7 Signal Assignment to Connector J3_9

This connector contains all ground referenced signals (general I/Os) of bank 7.

5.17 Signals on 0.1” Header Connectors

All signals of bank 0 and bank 1 that are not available on the differential connector J2_8 are routed to 0.1” header connectors J1_8 and J4_8. You can connect 26 wire ribbon cables to these headers or use them to connect oscilloscopes or logic analyzers. These header connectors are mainly intended for accessing monitor signals for test purposes.

5.18 Connection of several Boards

To facilitate the connection of external hardware or further Virtex-II boards, we created various ties and adapters for both single and differential signals. The ties provide point to point connections between Virtex-II boards with the possibility to connect oscilloscopes and logic analyzers, whereas the adapters enable you to connect ribbon cables to standard 0.1” header connectors.

6 Appendix A: Signals on ERmet® Connectors

The tables on the following pages show the connections of the general I/O FPGA pins to the ERmet® 2mm Hard Metric connectors.

ErSt Electronic GmbH
Aeschstrasse 171
CH-8123 Ebmatingen
Switzerland

Phone +41 1 980 61 44
Fax +41 1 980 61 30
Internet **info@erst.ch**
http://www.erst.biz
http://www.erst.ch

6.1 LVDS Signal Assignment to Connector J2_8

This connector is specially designed for differential signals. A maximum of 60 differential signal pairs are available.

Signal Name	J2_8 Pin	FF1152 Pin XC2V3000-8000	FF896 Pin XC2V1000-2000
IO_L25N_1	1	B6	
IO_L25P_1	2	B7	
IO_L67N_1	4	B11	
IO_L67P_1	5	B12	
IO_L22N_1	7	A4	
IO_L22P_1	8	A5	
IO_L28N_1	10	C7	A5
IO_L28P_1	11	C8	A6
IO_L73N_1	13	A11	
IO_L73P_1	14	A12	
IO_L49N_1	16	A6	
IO_L49P_1	17	A7	
IO_L30N_1	19	D9	B7
IO_L30P_1	20	C9	A7
IO_L72N_1	22	E13	C11(1)
IO_L72P_1	23	E14	C12(1)
IO_L24N_1	25	E8	C6
IO_L24P_1	26	E9	C7
IO_L29N_1	28	H12	F10
IO_L29P_1	29	H13	F11
IO_L26P_1	31	K12	H10
IO_L26N_1	32	J13	G11
IO_L60N_1	34	F11(3)	D9
IO_L60P_1	35	F12(3)	D10
IO_L74P_1	37	H14	F12(1)
IO_L74N_1	38	H15	F13(1)
IO_L53N_1	40	G12	E10
IO_L53P_1	41	G13	E11
IO_L71P_1	43	J14	G12(1)
IO_L71N_1	44	J15	G13(1)
IO_L52N_1	46	B9	
IO_L52P_1	47	B10	
IO_L50P_1	49	K13	H11
IO_L50N_1	50	K14	H12
IO_L79N_1	52	A13(3)	
IO_L79P_1	53	A14(3)	
IO_L54N_1	55	D10	B8
IO_L54P_1	56	D11	B9
IO_L92N_1	58	G16	E14(1) (5)
IO_L92P_1	59	G17	E15(1) (5)
IO_L84N_1	61	D14(3)	B12(1) (5)
IO_L84P_1	62	D15(3)	B13(1) (5)
IO_L68N_1	64	C11	A9(1)
IO_L68P_1	65	C12	A10(1)
IO_L80P_1	67	L16(3)	J14(1) (5)
IO_L80N_1	68	L17(3)	J15(1) (5)
IO_L83N_1	70	J17(3)	G15
IO_L83P_1	71	K17(3)	H15
IO_L76N_1	73	B13	
IO_L76P_1	74	B14	
IO_L78N_0	76	D20	B18(1) (5)
IO_L78P_0	77	D21	B19(1) (5)
IO_L71P_0	79	K20	H18(1)
IO_L71N_0	80	K21	H19(1)
IO_L78N_1	82	C13	A11(1) (5)
IO_L78P_1	83	C14	A12(1) (5)
IO_L68N_0	85	G22	E20(1)
IO_L68P_0	86	G23	E21(1)
IO_L30N_0	88	F23	D21
IO_L30P_0	89	F24	D22
IO_L70N_1	91	D12	B10(1)
IO_L70P_1	92	D13	B11(1)
IO_L23P_0	94	K22	H20
IO_L23N_0	95	K23	H21
IO_L05P_0	97	H24	F22
IO_L05N_0	98	H25	F23

Signal Name	J2_8 Pin	FF1152 Pin XC2V3000-8000	FF896 Pin XC2V1000-2000
IO_L54N_0	100	D22	B20
IO_L54P_0	101	D23	B21
IO_L82N_1	103	B17(3)	
IO_L82P_1	104	A17(3)	
IO_L25N_0	106	A30	
IO_L25P_0	107	A31	
IO_L76N_0	109	B21	
IO_L76P_0	110	B22	
IO_L93N_1	112	F16	D14
IO_L93P_1	113	F17	D15
IO_L77P_0	115	K15	H13(1) (5)
IO_L77N_0	116	K16	H14(1) (5)
IO_L72N_0	118	C22	A20(1)
IO_L72P_0	119	C23	A21(1)
IO_L74P_0	121	H20	F18(1)
IO_L74N_0	122	H21	F19(1)
IO_L77P_0	124	K19	H17(1) (5)
IO_L77N_0	125	J20	G18(1) (5)
IO_L53P_0	127	D24	B22
IO_L53N_0	128	C24	A22
IO_L73N_0	130	E21	C19(1)
IO_L73P_0	131	E22	C20(1)
IO_L50P_0	133	J21	G19
IO_L50N_0	134	J22	G20
IO_L60N_0	136	B25(3)	
IO_L60P_0	137	B26(3)	
IO_L70N_0	139	A23	
IO_L70P_0	140	A24	
IO_L29P_0	142	H22	F20
IO_L29N_0	143	H23	F21
IO_L28N_0	145	D25	B23
IO_L28P_0	146	D26	B24
IO_L67N_0	148	B23	
IO_L67P_0	149	B24	
IO_L20P_0	151	J23	G21
IO_L20N_0	152	J24	G22
IO_L49N_0	154	B28	
IO_L49P_0	155	B29	
IO_L26N_0	157	G24	E22
IO_L26P_0	158	G25	E23
IO_L06N_0	160	E26	C24
IO_L06P_0	161	F27	D25
IO_L22N_0	163	B30	
IO_L22P_0	164	B31	
IO_L24N_0	166	C26	A24
IO_L24P_0	167	D27	B25
IO_L52N_0	169	A26	
IO_L52P_0	170	B27	
IO_L19N_0	172	B32	
IO_L19P_0	173	C33	
IO_L02P_0	175	G26	E24
IO_L02N_0	176	H26	F24
IO_L01N_0	178	D29	B27
IO_L01P_0	179	C29	A27

Table 37: Differential connector pin to signal assignments. Pins marked with (1), (5), (3) are not available on the XC2V1000, XC2V1500 or XC2V3000, respectively.

6.2 Bank 2 Signal Assignment to Connector J3_8

This connector contains all ground referenced signals (general I/Os) of bank 2.

Signal Name	J3_8 Pin	FF1152 Pin XC2V3000-8000	FF896 Pin XC2V1000-2000
IO_L82N_2	1	U5(3)	R3
IO_L82P_2	2	T5(3)	P3
IO_L80P_2	3	U11(3)	R9(1) (5)
IO_L80N_2	4	T11(3)	P9(1) (5)
IO_L94N_2	5	U1	
IO_L84N_2	6	U4(3)	R2
IO_L84P_2	7	T4(3)	P2
IO_L96P_2	8	V4	T2
IO_L95P_2	9	U8	R6
IO_L95N_2	10	U9	R7
IO_L69N_2	11	N6	L4(1)
IO_L54N_2	12	N4	L2(1)
IO_L96N_2	13	U3	R1
IO_L74P_2	14	R9	N7(1)
IO_L74N_2	15	P9	M7(1)
IO_L54P_2	16	M4	K2(1)
IO_L93N_2	17	T6	P4
IO_L83P_2	18	U10(3)	R8
IO_L76N_2	19	R4	N2(1) (5)
IO_L94P_2	20	U2	
IO_L72N_2	21	P3	M1(1)
IO_L81N_2	22	R7(3)	N5(1) (5)
IO_L83N_2	23	T10(3)	P8
IO_L76P_2	24	P4	M2(1) (5)
IO_L91N_2	25	T2	
IO_L72P_2	26	N3	L1(1)
IO_L70N_2	27	P5	M3(1)
IO_L92N_2	28	U7	R5(1) (5)
IO_L71P_2	29	R10	N8(1)
IO_L91P_2	30	R1	
IO_L75N_2	31	P2	
IO_L70P_2	32	N5	L3(1)
IO_L92P_2	33	T7	P5(1) (5)
IO_L71N_2	34	P10	M8(1)
IO_L79N_2	35	P1(3)	
IO_L52N_2	36	M3	K1
IO_L29N_2	37	L7	J5
IO_L78N_2	38	T3	P1(1) (5)
IO_L50N_2	39	N7	L5
IO_L79P_2	40	N1(3)	
IO_L52P_2	41	L3	J1
IO_L29P_2	42	K7	H5
IO_L78P_2	43	R3	N1(1) (5)
IO_L50P_2	44	M7	K5
IO_L73N_2	45	M1	
IO_L53N_2	46	L4	J2
IO_L67N_2	47	M2	
IO_L77P_2	48	T8	P6(1) (5)
IO_L51N_2	49	L6	J4
IO_L73P_2	50	L1	
IO_L53P_2	51	K4	H2
IO_L67P_2	52	L2	
IO_L77N_2	53	R8	N6(1) (5)
IO_L44P_2	54	M8	K6
IO_L45N_2	55	J1	
IO_L49N_2	56	K2	
IO_L48N_2	57	L5	J3
IO_L68P_2	58	P8	M6
IO_L44N_2	59	L8	J6
IO_L43N_2	60	G1	
IO_L49P_2	61	J2	
IO_L48P_2	62	K5	H3
IO_L68N_2	63	N8	L6
IO_L26P_2	64	N10	L8
IO_L43P_2	65	F1	
IO_L46N_2	66	J3	G1

Signal Name	J3_8 Pin	FF1152 Pin XC2V3000-8000	FF896 Pin XC2V1000-2000
IO_L27N_2	67	J6	G4
IO_L47P_2	68	N9	L7
IO_L26N_2	69	M10	K8
IO_L19N_2	70	E1	
IO_L46P_2	71	H3	F1
IO_L22N_2	72	H6	F4
IO_L47N_2	73	M9	K7
IO_L05P_2	74	K9	H7
IO_L19P_2	75	D1	
IO_L30N_2	76	J4	G2
IO_L22P_2	77	G6	E4
IO_L23N_2	78	L10	J8
IO_L05N_2	79	J9	G7
not connected	80		
IO_L30P_2	81	H4	F2
IO_L24N_2	82	G3	E1
IO_L23P_2	83	L9	J7
not connected	84		
not connected	85		
IO_L25N_2	86	G2	
IO_L24P_2	87	F3	D1
IO_L20P_2	88	K8	H6
not connected	89		
not connected	90		
IO_L25P_2	91	F2	
IO_L06N_2	92	F4	D2
IO_L20N_2	93	J8	G6
not connected	94		
not connected	95		
IO_L03N_2	96	F5	D3
IO_L06P_2	97	E4	C2
IO_L28N_2	98	J5	G3
not connected	99		
not connected	100		
IO_L04N_2	101	E3	C1
IO_L01N_2	102	E2	
IO_L28P_2	103	H5	F3
not connected	104		
not connected	105		
IO_L04P_2	106	D3	B1
IO_L01P_2	107	D2	
IO_L21N_2	108	H7	F5
not connected	109		
not connected	110		
not connected	111		
not connected	112		
not connected	113		
not connected	114		
not connected	115		
1.5V	116		
2.5V/1.8V/1.5V	117		
3.3V	118		
GND	119		
GND	120		
1.5V	121		
2.5V/1.8V/1.5V	122		
3.3V	123		
GND	124		
GND	125		

Table 38: General I/Os of bank 2. Pins marked with (1), (5), (3) are not available on the XC2V1000, XC2V1500 or XC2V3000, respectively.

6.3 Bank 3 Signal Assignment to Connector J1_9

This connector contains all ground referenced signals (general I/Os) of bank 3.

Signal Name	J1_9 Pin	FF1152 Pin XC2V3000-8000	FF896 Pin XC2V1000-2000
not connected	1		
not connected	2		
not connected	3		
not connected	4		
not connected	5		
IO_L04P_3	6	AJ5	AG3
IO_L05P_3	7	AL2	
not connected	8		
not connected	9		
not connected	10		
IO_L04N_3	11	AH6	AF4
IO_L04N_3	12	AK2	
not connected	13		
not connected	14		
not connected	15		
IO_L20P_3	16	AJ2	
IO_L29P_3	17	AK4	AH2
not connected	18		
not connected	19		
not connected	20		
IO_L20N_3	21	AH2	
IO_L19N_3	22	AJ4	AG2
not connected	23		
not connected	24		
not connected	25		
IO_L25P_3	26	AH5(LCD)	AF3(LCD)
IO_L23P_3	27	AJ3(LCD)	AG1(LCD)
IO_L01N_3	28	AF10(LCD)	AD8(LCD)
IO_L01P_3	29	AG9	AE7
not connected	30		
IO_L25N_3	31	AG4(LCD)	AE2(LCD)
IO_L23N_3	32	AH3(LCD)	AF1(LCD)
IO_L03P_3	33	AF11(LCD)	AD9(LCD)
IO_L21P_3	34	AK1	
IO_L93P_3	35	W10	U8
IO_L43P_3	36	AG3(LCD)	AE1(LCD)
IO_L24P_3	37	AG6(LCD)	AE4(LCD)
IO_L22P_3	38	AG7(LCD)	AE5(LCD)
IO_L27P_3	39	AF9	AD7
IO_L26P_3	40	AJ1	
IO_L43N_3	41	AF3(LCD)	AD1(LCD)
IO_L24N_3	42	AF6(LCD)	AD4(LCD)
IO_L22N_3	43	AF7(LCD)	AD5(LCD)
IO_L45P_3	44	AE9	AC7
IO_L26N_3	45	AH1	
IO_L50P_3	46	AE5	AC3
IO_L49P_3	47	AF4	AD2
IO_L29P_3	48	AG5	AE3
IO_L30P_3	49	AE7	AC5
IO_L47P_3	50	AF1	
IO_L50N_3	51	AD5	AB3
IO_L49N_3	52	AE4	AC2
IO_L29N_3	53	AF5	AD3
IO_L30N_3	54	AD7	AB5
IO_L47N_3	55	AE2	
IO_L67P_3	56	AD4	AB2
IO_L46P_3	57	AE6	AC4
IO_L44P_3	58	AG2	
IO_L51P_3	59	AC10	AA8
IO_L69P_3	60	AC1	
IO_L67N_3	61	AC4	AA2
IO_L46N_3	62	AD6	AB4
IO_L44N_3	63	AF2	
IO_L75P_3	64	AA10	W8(1)
IO_L74P_3	65	AB1	
IO_L53P_3	66	AD2	
IO_L68P_3	67	AD3	AB1(1)
IO_L06N_3	68	AE10	AC8
IO_L77P_3	69	AB4	Y2(1) (5)
IO_L74N_3	70	AA1	
IO_L53N_3	71	AC2	
IO_L68N_3	72	AC3	AA1(1)
IO_L06P_3	73	AD10	AB8
IO_L77N_3	74	AA4	W2(1) (5)
IO_L80P_3	75	Y1(3)	
IO_L71P_3	76	AB2	
IO_L54P_3	77	AC7	AA5
IO_L28N_3	78	AE8	AC6
IO_L78P_3	79	AA6	W4(1) (5)
IO_L80N_3	80	W2(3)	
IO_L71N_3	81	AA2	
IO_L54N_3	82	AB7	Y5
IO_28P_3	83	AD8	AB6
IO_L78N_3	84	Y6	V4(1) (5)
IO_L92P_3	85	V2	
IO_L79P_3	86	AB3(3)	Y1(1) (5)
IO_L73P_3	87	AB5	Y3(1)
IO_L52N_3	88	AC8	AA6
IO_L81P_3	89	Y8(3)	V6(1) (5)
IO_L92N_3	90	V1	
IO_L79N_3	91	AA3(3)	W1(1) (5)
IO_L73N_3	92	AA5	W3(1)
IO_L52P_3	93	AB8	Y6
IO_L84N_3	94	V9(3)	T7
IO_L84P_3	95	V8(3)	T6
IO_L70P_3	96	AC6	AA4(1)
IO_L76P_3	97	AA8	W6(1)
IO_L48P_3	98	AC9	AA7
IO_L48N_3	99	AB9	Y7
IO_L82N_3	100	W11(3)	U9(1) (5)
IO_L70N_3	101	AB6	Y4(1)
IO_L76N_3	102	Y7	V5(1)
IO_L72N_3	103	AA9	W7(1)
IO_L72P_3	104	Y9	V7(1)
IO_L82P_3	105	V11(3)	T9(1) (5)
IO_L83P_3	106	Y4(3)	V2
IO_L83N_3	107	W4(3)	U2
IO_L96P_3	108	W6	U4
IO_L91P_3	109	Y3	V1
IO_L91N_3	110	W3	U1
IO_L95P_3	111	W5	U3
IO_L95N_3	112	V5	T3
IO_L96N_3	113	V6	T4
IO_L94P_3	114	W7	U5(1) (5)
IO_L94N_3	115	V7	T5(1) (5)
1.5V	116		
2.5V/1.8V/1.5V	117		
3.3V	118		
GND	119		
GND	120		
1.5V	121		
2.5V/1.8V/1.5V	122		
3.3V	123		
GND	124		
GND	125		

Table 39: General I/Os of bank 3. Pins marked with (1), (5), (3) are not available on the XC2V1000, XC2V1500 or XC2V3000, respectively. Pins marked with (LCD) are also connected with the LCD module, see paragraph 5.12.

6.4 Bank 6 Signal Assignment to Connector J2_9

This connector contains all ground referenced signals (general I/Os) of bank 6.

Signal Name	J2_9 Pin	FF1152 Pin XC2V3000-8000	FF896 Pin XC2V1000-2000
IO_L95N_6	1	V30	T28
IO_L84N_6	2	V29(3)	T27
IO_L82P_6	3	W25(3)	U23
IO_L82N_6	4	V25(3)	T23
IO_L79N_6	5	V24(3)	T22(1) (5)
IO_L95P_6	6	W30	U28
IO_L84P_6	7	W29(3)	U27
IO_L91P_6	8	W28	U26(1)(5)
IO_L91N_6	9	V28	T26(1) (5)
IO_L79P_6	10	W24(3)	U22(1)(5)
IO_L96P_6	11	V32	T30
IO_L54N_6	12	AA27	W25
IO_L70P_6	13	AA26	W24(1)
IO_L70N_6	14	Y26	V24(1)
IO_L94N_6	15	V27	T25
IO_L96N_6	16	W32	U30
IO_L54P_6	17	AB27	Y25
IO_L83N_6	18	AA32(3)	W30(1) (5)
IO_L83P_6	19	Y32(3)	V30(1) (5)
IO_L94P_6	20	V26	T24
IO_L93P_6	21	Y31	V29
IO_L78P_6	22	AA30	W28(1)
IO_L49N_6	23	AB26	Y24
IO_L73P_6	24	Y27	V25(1) (5)
IO_L73N_6	25	W27	U25(1) (5)
IO_L74N_6	26	AA29	W27(1)
IO_L78N_6	27	AB30	Y28(1)
IO_L49P_6	28	AC26	AA24
IO_L66P_6	29	Y28	V26(1) (5)
IO_L76N_6	30	Y29	V27(1) (5)
IO_L74P_6	31	AB29	Y27(1)
IO_L50N_6	32	AC29	AA27
IO_L52N_6	33	AB28	Y26(1)
IO_L67N_6	34	Y25	V23(1)
IO_L75P_6	35	AB31	Y29(1) (5)
IO_L77N_6	36	AA33	
IO_L50P_6	37	AD29	AB27
IO_L52P_6	38	AC28	AA26(1)
IO_L43N_6	39	AB25	Y23
IO_L67P_6	40	AA25	W23(1)
IO_L77P_6	41	AB33	
IO_L72P_6	42	AC31	AA29
IO_L46N_6	43	AC27	AA25
IO_L27P_6	44	AE28	AC26
IO_L43P_6	45	AC25	AA23
IO_L68N_6	46	AC33	
IO_L72N_6	47	AD31	AB29
IO_L46P_6	48	AD27	AB25
IO_L28N_6	49	AD26	AB24
IO_L92N_6	50	V34	
IO_L68P_6	51	AD33	
IO_L45P_6	52	AE31	AC29
IO_L25N_6	53	AE27	AC25
IO_L28P_6	54	AE26	AC24
IO_L92P_6	55	V33	
IO_L69P_6	56	AC32	AA30(1)
IO_L24N_6	57	AE29	AC27
IO_L25P_6	58	AF27	AD25
IO_L04N_6	59	AE25	AC23
IO_L81P_6	60	W33(3)	
IO_L48N_6	61	AD30	AB28
IO_L24P_6	62	AF29	AD27
IO_L51P_6	63	AF33	
IO_L04P_6	64	AF25	AD23
IO_L80N_6	65	AA34(3)	
IO_L48P_6	66	AE30	AC28

Signal Name	J2_9 Pin	FF1152 Pin XC2V3000-8000	FF896 Pin XC2V1000-2000
IO_L06P_6	67	AH29	AF27
IO_L06N_6	68	AG29	AE27
IO_L29P_6	69	AF31	AD29
IO_L80P_6	70	AB34(3)	
IO_L30P_6	71	AF32	AD30
IO_L05P_6	72	AJ31	AG29
IO_L21P_6	73	AJ32	AG30
IO_L29N_6	74	AG31	AE29
IO_L71N_6	75	AC34	
IO_L30N_6	76	AG32	AE30
IO_L05N_6	77	AK31	AH29
IO_L22N_6	78	AF28	AD26
IO_L71P_6	79	AD34	
not connected	80		
IO_L23N_6	81	AF30	AD28
IO_L20N_6	82	AK33	
IO_L53N_6	83	AE33	
not connected	84		
not connected	85		
IO_L23P_6	86	AG30	AE28
IO_L20P_6	87	AL33	
IO_L53P_6	88	AF34	
not connected	89		
not connected	90		
IO_L44N_6	91	AH33	
IO_L19N_6	92	AF26	AD24
IO_L47N_6	93	AH34	
not connected	94		
not connected	95		
IO_L44P_6	96	AJ33	
IO_L19P_6	97	AG26	AE24
IO_L47P_6	98	AJ34	
not connected	99		
not connected	100		
IO_L03P_6	101	AL32	AJ30
IO_L22P_6	102	AG28	AE26
IO_L26N_6	103	AK34	
not connected	104		
not connected	105		
IO_L01P_6	106	AE24	AC22
IO_L01N_6	107	AD25	AB23
IO_L26P_6	108	AL34	
not connected	109		
not connected	110		
not connected	111		
not connected	112		
not connected	113		
not connected	114		
not connected	115		
1.5V	116		
2.5V/1.8V/1.5V	117		
3.3V	118		
GND	119		
GND	120		
1.5V	121		
2.5V/1.8V/1.5V	122		
3.3V	123		
GND	124		
GND	125		

Table 40: General I/Os of bank 6. Pins marked with (1), (5), (3) are not available on the XC2V1000, XC2V1500 or XC2V3000, respectively.

6.5 Bank 7 Signal Assignment to Connector J3_9

This connector contains all ground referenced signals (general I/Os) of bank 7.

Signal Name	J3_9 Pin	FF1152 Pin XC2V3000-8000	FF896 Pin XC2V1000-2000
IO_L06P_7	1	D32	B30
IO_L01P_7	2	D33	
IO_L20N_7	3	J26	G24
IO_L21N_7	4	J27	G25
IO_L04P_7	5	D34	
IO_L06N_7	6	E32	C30
IO_L01N_7	7	E33	
IO_L20P_7	8	K27	H25
IO_L29N_7	9	M25	K23
IO_L04N_7	10	E34	
IO_L03N_7	11	F30	D28
IO_L19P_7	12	E31	C29
IO_L27N_7	13	H30	F28
IO_L29P_7	14	N25	L23
IO_L28P_7	15	F34	
IO_L22P_7	16	F33	
IO_L19N_7	17	F31	D29
IO_L23N_7	18	K26	H24
IO_L44N_7	19	L27	J25
IO_L28N_7	20	G34	
IO_L22N_7	21	G33	
IO_L30P_7	22	F32	D30
IO_L23P_7	23	L26	J24
IO_L44P_7	24	M27	K25
IO_L45N_7	25	J34	
IO_L43P_7	26	H31	F29
IO_L30N_7	27	G32	E30
IO_L54P_7	28	L31	J29
IO_L51N_7	29	L29	J27
IO_L70P_7	30	L34	
IO_L43N_7	31	J31	G29
IO_L24P_7	32	G29	E27
IO_L54N_7	33	M31	K29
IO_L50P_7	34	M28	K26
IO_L70N_7	35	M34	
IO_L48P_7	36	H32	F30
IO_L24N_7	37	H29	F27
IO_L47N_7	38	M26	K24
IO_L50N_7	39	N28	L26
IO_L81N_7	40	P34(3)	
IO_L48N_7	41	J32	G30
IO_L25P_7	42	H28	F26
IO_L47P_7	43	N26	L24
IO_L71N_7	44	P25	M23(1)
IO_L82P_7	45	R34(3)	
IO_L46P_7	46	J33	
IO_L25N_7	47	J29	G27
IO_L68N_7	48	N27	L25
IO_L71P_7	49	R25	N23(1)
IO_L82N_7	50	T33(3)	
IO_L46N_7	51	K33	
IO_L53P_7	52	K29	H27
IO_L68P_7	53	P27	M25
IO_L74N_7	54	P26	M24(1)
IO_L94P_7	55	U33	
IO_L49N_7	56	K31	H29
IO_L53N_7	57	L30	J28
IO_L84P_7	58	R32(3)	N30
IO_L74P_7	59	R26	N24(1)
IO_L94N_7	60	U34	
IO_L49P_7	61	K30	H28
IO_L52P_7	62	L33	
IO_L84N_7	63	T32(3)	P30
IO_L79P_7	64	R31(3)	N29(1) (5)
IO_L05N_7	65	K24	H22
IO_L67P_7	66	L32	J30(1)
IO_L52N_7	67	M33	
IO_L95P_7	68	T28	P26(1) (5)
IO_L79N_7	69	T31(3)	P29(1) (5)
IO_L05P_7	70	L25	J23
IO_L67N_7	71	M32	K30(1)
IO_L26P_7	72	K28	H26
IO_L95N_7	73	U28	R26(1) (5)
IO_L92N_7	74	U26	R24
not connected	75		
IO_L76P_7	76	N33	
IO_L26N_7	77	L28	J26
IO_L83N_7	78	T25(3)	P23
IO_L92P_7	79	U27	R25
not connected	80		
IO_L76N_7	81	P33	
IO_L72P_7	82	N30	L28(1)
IO_L83P_7	83	U25(3)	R23
IO_L80N_7	84	T24(3)	P22(1) (5)
not connected	85		
IO_L78P_7	86	N32	L30(1) (5)
IO_L72N_7	87	P30	M28(1)
IO_L80P_7	88	U24(3)	R22(1) (5)
not connected	89		
not connected	90		
IO_L73P_7	91	N31	L29(1)
IO_L78N_7	92	P32	M30(1) (5)
IO_L77N_7	93	R27	N25(1) (5)
not connected	94		
not connected	95		
IO_L69N_7	96	N29	L27(1)
IO_L73N_7	97	P31	M29(1)
IO_L77P_7	98	T27	P25(1) (5)
not connected	99		
not connected	100		
IO_L91P_7	101	T30	P28
IO_L75N_7	102	R28	N26(1) (5)
IO_L93N_7	103	T29	P27
not connected	104		
not connected	105		
IO_L91N_7	106	U30	R28
IO_L96N_7	107	V31	T29
IO_L96P_7	108	U31	R29
not connected	109		
not connected	110		
not connected	111		
not connected	112		
not connected	113		
not connected	114		
not connected	115		
1.5V	116		
2.5V/1.8V/1.5V	117		
3.3V	118		
GND	119		
GND	120		
1.5V	121		
2.5V/1.8V/1.5V	122		
3.3V	123		
GND	124		
GND	125		

Table 41: General I/Os of bank 7. Pins marked with (1), (5), (3) are not available on the XC2V1000, XC2V1500 or XC2V3000, respectively.

6.6 Signals on 0.1" Header Connectors

6.6.1 Remaining Signals of Bank 0 and 1

All signals that are not routed to the differential connector J2_8 are available on 0.1" header connectors. Signal integrity may not be as high as on the other connectors. These signals should be used as debugging and monitoring signals.

The pin assignments are listed in the following tables:

Signal Name	J1_8 Pin	FF1152 Pin XC2V3000-8000	FF896 Pin XC2V1000-2000
IO_L01P_1	1	B3	
IO_L01N_1	2	C2	
IO_L21P_1	3	G9	E7
IO_L51P_1	4	A9	
IO_L91N_1	5	C16	A14
IO_L75P_1	6	G15	E13 (1) (5)
IO_L94N_1	7	D17	B15
IO_L20N_1	8	J12	G10
IO_L20P_1	9	J11	G9
IO_L69P_1	10	F13	D11 (1)
IO_L81P_1	11	B16 (3)	
IO_L82N_0	12	A18 (3)	
IO_L82P_0	13	B18 (3)	
IO_L81N_0	14	B19 (3)	
IO_L94P_0	15	C18	A16
IO_L80N_0	16	L19 (3)	J17 (1) (5)
IO_L84P_0	17	C21 (3)	A19 (1) (5)
IO_L79N_0	18	A21 (3)	
IO_L79P_0	19	A22 (3)	
IO_L27N_0	20	E25	C23
IO_L04P_0	21	F26	D24
IO_L21N_0	22	C27	A25
IO_L51N_0	23	A28	
3.3V	24		
GND	25		
GND	26		

Table 42: Bank 0 and 1 signals on header connectors J1_8. Pins marked with (1), (5), (3) are not available on the XC2V1000, XC2V1500 or XC2V3000, respectively.

Signal Name	J4_8 Pin	FF1152 Pin XC2V3000-8000	FF896 Pin XC2V1000-2000
IO_L19N_1	1	B4	
IO_L19P_1	2	B5	
IO_L02P_1	3	H9	F7
IO_L02N_1	4	H10	F8
IO_L05P_1	5	J10	G8
IO_L05N_1	6	H11 (TTSP)	F9 (TTSP)
IO_L06N_1	7	D6 (TTSP)	B4 (TTSP)
IO_L06P_1	8	C6 (TTSP)	A4 (TTSP)
IO_L04N_1	9	D8 (TTSP)	B6 (TTSP)
IO_L23P_1	10	G11 (TTSP)	E9 (TTSP)
IO_L27P_1	11	E10 (TTSP)	C8 (TTSP)
IO_L83N_0	12	H19 (3)	F17
IO_L83P_0	13	H18 (3)	F16
IO_L91P_0	14	D18 (TTSP)	B16 (TTSP)
IO_L92P_0	15	G19	E17 (1) (5)
IO_L92N_0	16	G18	E16 (1) (5)
IO_L93P_0	17	F19 (TTSP)	D17 (TTSP)
IO_L93N_0	18	F18 (TTSP)	D16 (TTSP)
IO_L84N_0	19	C20 (3)	A18 (1) (5)
IO_L80P_0	20	L18 (3)	J16 (1) (5)
IO_L75N_0	21	G20	E18 (1) (5)
IO_L69N_0	22	F22	D20 (1)
3.3V	23		
3.3V	24		
GND	25		
GND	26		

Table 43: Bank 0 and 1 signals on header connectors J4_8. Pins marked with (1), (5), (3) are not available on the XC2V1000, XC2V1500 or XC2V3000, respectively. Pins marked with (TTSP) also connect to the text-to-speech processor if the jumpers J3_11 and J7_11 are inserted.

6.7 Total Number of General I/Os on External Connectors

The following table summarizes the total number of general I/Os available on the external connectors for the different FPGA device types.

FPGA Device (Package)	LVDS Pairs Bank 0, 1	Bank 2	Bank 3	Bank 6	Bank 7	Total (Banks 2, 3, 6 & 7)	Total (Banks 0, 1, 2, 3, 6 & 7)
XC2V1000 (FF896)	25	53	53	53	53	212	262
XC2V1500 (FF896)	35	64	65	64	64	257	327
XC2V2000 (FF896)	42	75	75	75	75	300	384
XC2V3000 (FF1152)	53	87	86	86	87	346	452
XC2V4000 (FF1152)	60	97	97	97	97	388	508
XC2V6000 (FF1152)	60	97	97	97	97	388	508
XC2V8000 (FF1152)	60	97	97	97	97	388	508

Table 44: Overview of maximal available general I/Os on external connectors.

7 Appendix B: Literature

7.1 Datasheets of Peripheral Components

Analog Devices, http://www.analog.com
- ADM1021A, System Temperature Monitor

MAXIM, http://www.maxim-ic.com
- MAX1617, Remote/Local Temperature Sensor with SMBus Serial Interface
- MAX3221, ±15kV ESD-Protected, 250kbps, RS-232 Transceivers

National Semiconductor, http://www.national.com
- DS26LV31T, RS-422 Differential Line Driver
- DS26LV32AT, RS-422 Differential Line Receiver
- LM4861, Audio Power Amplifier
- LM4901, Audio Power Amplifier

Samsung Electronics, http://www.microtipsusa.com/products/drivers.html
- KS0073, 34COM / 60SEG Driver & Controller for Dot Matrix LCD
- K6R4016V1D, 256Kx16 Bit High Speed Static RAM (3.3V Operating)

Seiko Epson Corporation, http://www.epson.co.jp/device/
- Application Manual: Real Time Clock Module RTC-8564
- I^2C-Bus Interface Real Time Clock Module RTC-8564JE/NB

Texas Instruments, http://www.ti.com
- TLC7701, Micropower Supply Voltage Supervisor

Winbond, http://www.winbond-usa.com
- WTS701, Single-Chip Text-to-Speech Processor

ERNI, http://www.erni.com
- Main board connector for ground referenced signals: 114538
- Adapter board connector ground referenced signals: 114153
- Main board connector for differential signals: 973028
- Adapter board connector for differential signals: 973027

Radiall, http://www.radiall.com
- Coaxial connectors: R 114 426

7.2 Xilinx Literature

Application Notes: Virtex, Virtex-E and Virtex-II, http://www.xilinx.com/apps/virtexapp.htm

- XAPP649: SONET Rate Conversion in Virtex-II Pro Devices
- XAPP632: Programming an FPGA via E-mail
- XAPP626: High-Speed Interface with a Velio SerDes
- XAPP625: SDI: Video Standard Detector and Flywheel Decoder
- XAPP622: 644-MHz SDR LVDS Transmitter/Receiver
- XAPP611: Video Compression Using IDCT
- XAPP610: Video Compression Using DCT
- XAPP607: Virtex-II Connection to a High Speed Serial Device (TLK2501)
- XAPP606: XGMII Using the DDR Registers, DCM, and SelectI/O Features in Virtex-II Devices
- XAPP299: SDI: Ancillary Data and EDH Processors
- XAPP298: SDI: Video Encoder
- XAPP291: Self-Addressing FIFO
- XAPP290: Two Flows for Partial Reconfiguration: Module Based or Small Bit Manipulations
- XAPP289: Common Switch Interface CSIX-L1
- XAPP288: SDI: Video Decoder
- XAPP284: 3x3 Matrix Multiplier for 3D Graphics and Video
- XAPP283: Color Space Converter
- XAPP270: High-Speed DES and Triple DES Encryptor / Decryptor
- XAPP268: Active Phase Alignment
- XAPP267: Parity Generation and Validation in Virtex-II Devices
- XAPP266: Synthesizable FCRAM Controller
- XAPP265: High-Speed Data Serialization and Deserialization (840 Mb/s LVDS)
- XAPP262: Quad DataRate (QDR) SRAM Interface for Virtex-II Devices
- XAPP261: Data-Width Conversion FIFOs Using the Virtex-II Block RAM Memory
- XAPP260: Using Virtex-II Block RAM for High-Performance Read/Write CAMs
- XAPP258: FIFOs Using Virtex-II Block RAM
- XAPP256: FIFOs Using Virtex-II Shift Registers
- XAPP254: The Virtex-II SiberBridge
- XAPP253: Synthesizable 266 MBits/s DDR SDRAM Controller
- XAPP251: Hot-Swapping Virtex-II Devices
- XAPP250: Clock and Data Recovery With Coded Data Streams
- XAPP248: Digital Video Test Pattern Generators
- XAPP246: PowerPC 60X Bus Interface to a Virtex-E
- XAPP245: Eight Channel, One Clock, One Frame LVDS Transmitter/Receiver
- XAPP243: Bus LVDS with Virtex-E Devices
- XAPP242: Interfacing to Lara Networks Search Engine using Virtex Devices
- XAPP241: Virtex-EM FIR Filter for Video Applications
- XAPP240: High-Speed Buffered Crossbar Switch Design using Virtex-EM Devices
- XAPP238: LVDS System Data Framing
- XAPP237: Virtex-E LVPECL Receivers in Multi-Drop Applications
- XAPP235: Virtex-E Package Compatibility Guide
- XAPP234: Virtex SelectLink Communications Channel
- XAPP233: Multi-channel 622 Mb/s LVDS Data Transfer with Virtex-E Devices
- XAPP232: Virtex-E LVDS Drivers and Receivers: Interface Guidelines
- XAPP230: The LVDS I/O Standard
- XAPP225: Data to Clock Phase Alignment
- XAPP224: Data Recovery
- XAPP223: 200MHz UART with Internal 16-Byte Buffer
- XAPP222: Designing Convolutional Interleavers with Virtex Devices
- XAPP220: Linear Feedback Shift Registers for Wireless Applications
- XAPP219: Transposed Form FIR Filters
- XAPP217: Gold Code Generators in Virtex Devices
- XAPP216: Correcting Single-Event Upsets Through Virtex Partial Reconfiguration
- XAPP215: Design Tips for HDL Implementation of Arithmetic Functions
- XAPP214: Virtex Device Quad Data Rate (QDR) SRAM Interface
- XAPP213: PicoBlaze 8-Bit Microcontroller for Virtex Devices
- XAPP212: CDMA Matched Filters Implementation in Virtex Devices
- XAPP211: PN Generators Using the Virtex SRL Macro

- XAPP210: Linear Feedback Shift Registers in Virtex Devices
- XAPP209: IEEE 802.3 Cyclic Redundancy Check
- XAPP208: IDCT implementation in Virtex Devices for MPEG applications
- XAPP205: Data-Width Conversion FIFOs using Virtex Block SelectRAM Memory
- XAPP204: CAM in Block Select RAM
- XAPP203: Designing Flexible, Fast CAMs with Virtex Slices
- XAPP202: CAM in ATM applications
- XAPP201: An Overview of Multiple CAM Designs in Virtex Devices
- XAPP200: Double Data Rate SDRAM
- XAPP198: Synthesizable FPGA Interface for Retrieving ROM Number from 1-Wire Devices
- XAPP196: Interfacing a Virtex-E Device to a Pentium Processor
- XAPP192: Interfacing a Virtex-E Device to a MIPS Processor
- XAPP158: Powering Virtex FPGAs
- XAPP155: Virtex Analog to Digital Converter
- XAPP154: Virtex Synthesizable Delta-Sigma DAC
- XAPP153: Status and Control Semaphore Registers Using Partial Reconfiguration
- XAPP152: Virtex Power Estimator User Guide
- XAPP151: Virtex Configuration Architecture Advanced User Guide
- XAPP139: Virtex Configuration and Readback through Boundary Scan
- XAPP138: Virtex Configuration and Readback
- XAPP137: Configuring Virtex FPGAs from Parallel EPROMs with a CPLD
- XAPP136: Synthesizable 200 MHz ZBT(TM) SRAM Interface
- XAPP135: Virtex I/V Curves for Various Output Options
- XAPP134: Virtex Synthesizable High Performance SDRAM Controller
- XAPP133: Using the Virtex SelectI/O Resource
- XAPP132: Using the Virtex Delay-Locked Loop
- XAPP131: 170MHz Synchronous and Asynchronous FIFOs Using the Virtex Block SelectRAM+ Features
- XAPP130: Using the Virtex Block SelectRAM+

- Virtex-II 1.5V Platform FPGA Data Sheet
- Virtex-II Platform FPGA Handbook

8 Appendix C: PCB Layout, Mechanical Drawing and Schematic Diagram

PCB layout, mechanical drawings and schematic diagrams are only present in the printed manual but are available on request.

The following pages show the technical details of the board:

- Top overlay silk screen and top layer
- Mid layers
- Bottom overlay silk screen and bottom layer
- Mechanical drawing
- Schematic diagram

The ground planes and the supply voltage planes are not shown.